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ORIGINAL ARTICLE

AN OVERVIEW OF RADIATION EFFECTS IN ELECTRONICS

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ABSTRACT:

Energetic particle radiation significantly influences the functionality and longevity of electronic devices within radiation-prone environments. This paper aims to introduce the prevalent radiation effects encountered in microelectronics, along with commonly employed strategies for mitigation.

INTRODUCTION

Radiation effects in microelectronics pose significant challenges for device performance and durability in diverse radiation environments, spanning from outer space and aircraft avionics to accelerators, nuclear power plants, and critical ground-level equipment. This overview aims to cover the various mechanisms of radiation effects and prevalent mitigation strategies. For more detailed insights into these effects and testing methodologies, comprehensive resources are available in several authoritative books [1-3].

TYPES OF RADIATION EFFECTS

Radiation effects in microelectronics can be categorized into several groups. The primary distinction lies in whether the effect arises from the cumulative damage caused by numerous energetic particles or from the impact of a single particle. Cumulative damage examples encompass total ionizing dose (TID) and displacement damage dose (DDD). Failures attributed to a single particle can either be destructive or non-destructive to the device, and include memory upsets, latchup, gate rupture, burnout, and other phenomena collectively known as single event effects (SEE).

Total Ionizing Dose

Figure 1 depicts the operation of a metal-on-silicon (MOS) transistor [4], which is among the most common electronic components forming the foundation of digital logic. In an NMOS (negative carrier) device, electrons in the source are initially isolated from the drain contact. Applying a positive charge to the gate lowers the potential barrier, enabling electrons to tunnel from the source to the drain.

When ionizing radiation penetrates the device, electrons are liberated from the material's atoms, leaving behind positively charged "holes." Electrons are swiftly driven out by electric fields, but holes, less mobile, hop between atoms within the crystal lattice. Some holes may reach the gate oxide and become trapped there. This accumulation of trapped charge at interfaces within the device is known as "total ionizing dose." The consequence mimics the effect of applying a positive gate voltage in normal operation, eventually causing the transistor to remain

in the ON state due to sufficient accumulated charge. Conversely, for PMOS (positive charge carriers), this process shifts the device toward the OFF state.

Charge trapping is not limited to the gate oxide in electronic devices; it can occur in various locations within the device structure. Figure 2 illustrates that many devices feature numerous transistors separated by a field oxide. Accumulated charge on the field oxide can form a conductive channel that links adjacent transistors together. This phenomenon significantly impacts the operation of individual nodes and the overall circuit performance. Additionally, defects within the crystal lattice and other boundaries within the device can also serve as sites where charge becomes trapped, further influencing device behavior. For a more detailed exploration of the fundamental physical mechanisms underlying ionizing radiation interactions with MOS oxides, refer to [5].

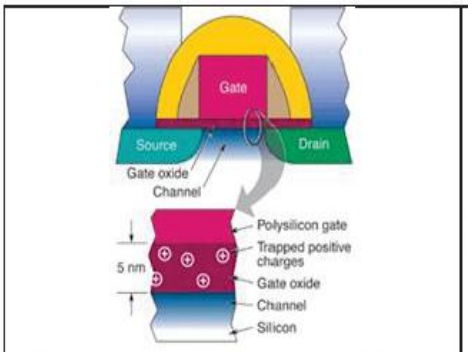

Figure 1: Charged particles ionize the gate oxide. Trapped holes build up an effective positive voltage on the gate that keeps the device ON (NMOS) or OFF (PMOS).

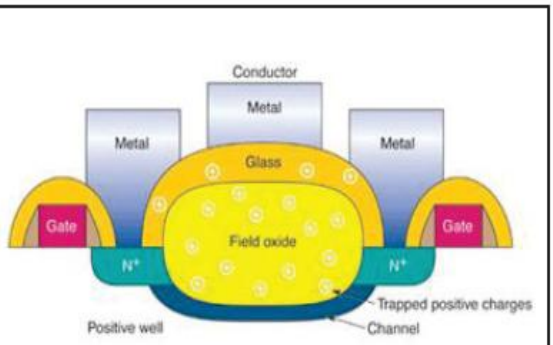

Figure 2: Trapped charge in a field oxide forms a conducting channel between formerly isolated NMOS transistors.

Displacement Damage Dose

Another type of cumulative damage results from induced dislocations in the crystal lattice, termed displacement damage dose (DDD) [5,6]. In Figure 3, a particle, typically a proton or neutron, displaces an atom from its position within the crystal lattice, creating a vacancy and an interstitial in the material's structure. These microscopic defects serve as traps and recombination centers, altering the electronic band structure and hindering the flow of charge across the device. The deceleration of the incident particle due to atomic collisions is often referred to as "non-ionizing energy loss" (NIEL). However, the recoiling atoms or atomic fragments, if the collision energy is sufficiently high, are usually charged and can also deposit ionizing dose.

Figure 4 illustrates the operation of a bipolar junction transistor (BJT), which acts as a current amplifier. Electrons emitted from the emitter region diffuse through the base to reach the collector. Defects within the base region function as recombination centers, reducing the electron flow through the base and consequently lowering the amplifier's gain. This decrease in gain directly impacts the circuit's performance that relies on this parameter. This example underscores that radiation effects extend beyond digital logic, affecting linear circuits as well.

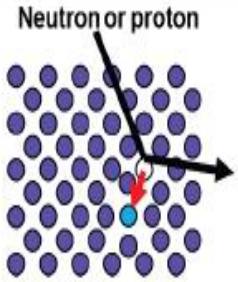

Figure 3: Atomic collisions between energetic particles and atoms in the crystal lattice create microscopic defects that affect device performance.

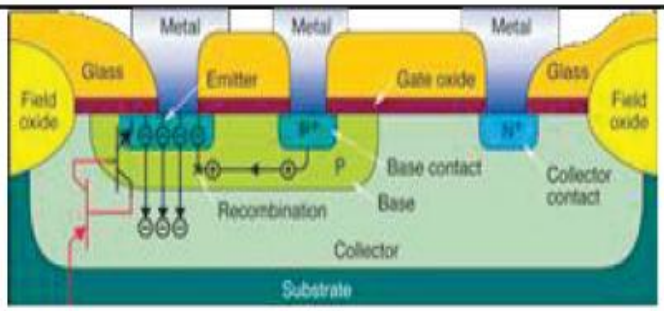

Figure 4: Recombination centers from trapped charge in the base region of a bipolar junction transistor reduce the flow of electrons from the emitter to the collector.

Single Event Effects

Unlike total ionizing dose and displacement damage, which accumulate over time from multiple incident particles, single event effects (SEE) result from the passage of a single charged particle through the device, as depicted in Figure 5. As mentioned earlier, the charged particle ionizes atoms along its path, releasing electrons and holes as charge carriers. In the presence of an electric field, electrons are quickly swept away before they can recombine with the holes, allowing both carriers to contribute to current at the circuit nodes. Essentially, the particle injects a transient pulse of charge through the device. This sudden charge spike manifests as an unexpected current that can impact the device in various ways [3].

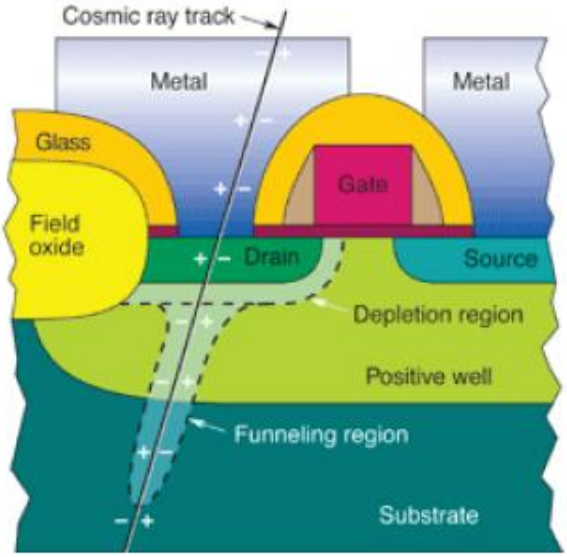

Figure 5: A single charged particle passing through a trans is torionizes the a toms along its path, creating electronhole pairs. The electrons may be collected atthedrain, placing charge where it was not expected.

Destructive Single Event Effects

Some single event effects can lead to catastrophic device failure, while others can degrade performance to the extent that it no longer meets the circuit's required tolerances.

These effects are collectively referred to as destructive single event effects (SEE). The most common types include single event latchup (SEL), single event burnout (SEB), and single event gate rupture or dielectric rupture (SEGR/SEDR).

Single event latchup occurs when the path of a charged particle activates a parasitic transistor, as depicted in Figure 6. These parasitic transistors exist due to adjacent n- and p-doped regions in neighboring transistors. When a charged particle activates this parasitic structure, a positive feedback loop initiates, potentially escalating current flow to the limits of the power supply or causing device destruction. The feedback loop persists until the bias voltage drops below a certain holding threshold. In some cases, circuit path resistance may limit current to non-damaging levels, categorized as non-destructive. However, normal operation recovery often requires a power cycle, and concerns about latent damage that could manifest later remain.

Single event burnout occurs when charge accumulation in a region of high electric field triggers secondary breakdown, initiating an avalanche effect that multiplies charges. This scenario can lead to thermal runaway, resulting in localized melting or expulsion of molten material—a small-scale explosion. Typically, this results in complete device failure. Figure 7 illustrates such an event occurring along the edge of a guard ring in a Schottky diode [7].

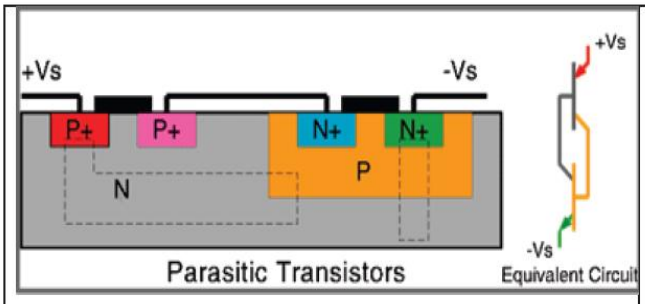

Figure 6: Single event latchup occurs when a particle turns on a parasitic transistor connecting two adjacent nodes through the substrate. This initiates a positive feedback that continues until power is removed or the device is destroyed.

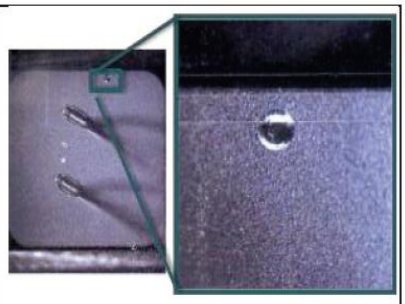

Figure 7: Single event burnout in a Schottky diode. An incident particle initiates an avalanche multiplication process that leads to thermal runaway.

Non-destructive Single Event Effects

Some single event effects do not cause outright device failure but still disrupt normal operation. Among the most recognized of these effects is the single event upset (SEU), commonly referred to as a "bit-flip" in a memory cell. Figure 8 illustrates a simplified static random-access memory (SRAM) cell composed of cross-coupled transistors. Initially, transistors Q1 and Q4 are OFF while Q2 and Q3 are ON, representing a "0" bit, for instance. If an ion strike occurs on Q1, it turns ON momentarily, closing the switch. This action pulls the gate of Q4 high, turning it ON as well, thereby pulling down the gates of Q3 and Q4. As a result, the cell settles into the opposite configuration, now representing a "1". The circuit continues to operate normally, but the stored data has changed.

Charge accumulation at a node can also manifest as an analog signal known as a single event transient (SET). These voltage spikes, as depicted in Figure 9 for example, can propagate through the circuit and affect downstream components. Devices with sensitive inputs may be damaged by spikes originating from prior stages. Transients can also traverse through combinational logic and be captured as a digital upset when latched into a register at a clock edge. The rate of single event transients in such circuits typically increases linearly with clock frequency, as faster clocks provide more opportunities for glitches to be registered as incorrect logic states.

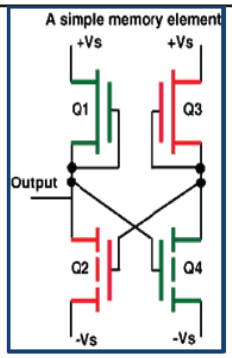

Figure 8: Simplified diagram of a basic memory storage cell. An ion strike on Q1 puts a momentary pulse on Q2 and Q4 that ultimately flips the logic state of the cell.

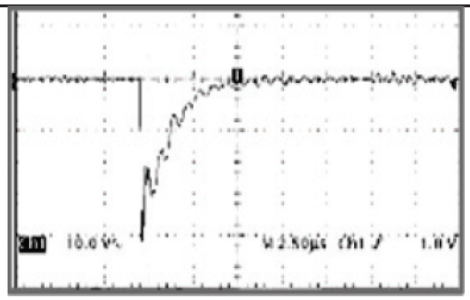

Figure 9: Single event transients can appear at the outputs of struck devices. These spikes can propagate through the circuit to affect downstream components. They can also produce clock glitches or be latched into digital logic as erroneous data.

Directvs.Indirect Ionization

Heavy ions, which encompass all atomic nuclei heavier than hydrogen, primarily interact with devices through direct ionization. These particles deposit sufficient charge in sensitive volumes to affect device performance directly. In contrast, protons are lightly ionizing and typically do not deposit enough charge to directly impact devices in most cases. Instead, they can collide with atomic nuclei within the device material, ejecting recoil ions or ion fragments into the sensitive region. These secondary particles are often heavier and ionize strongly enough to cause device effects in a conventional manner.

The likelihood of errors induced through this indirect process is significantly lower than those caused by direct ionization from heavier ions, due to the additional factor of the nuclear scattering cross section. This cross section represents the probability that an initial proton will interact with a nucleus in the device material, typically ranging from 10^-4 to 10^-5. This factor adds to the already low probability that the recoil ions or fragments from the initial proton will actually induce an error in the device. However, in certain environments such as Earth's trapped radiation belts or specific accelerator locations, the sheer abundance of protons can outweigh their lower individual probability, making proton-initiated events the predominant source of device errors.

Neutrons exhibit similar interactions to protons when it comes to producing single event effects in devices. Unlike protons, neutrons are uncharged and thus do not contribute to direct ionization. However, they can undergo nuclear collisions in a manner similar to protons. Neutrons in the 50-100 MeV energy range have scattering cross sections comparable to those of protons.

"Fast" neutrons, with energies down to about 1 MeV, can generate recoil ions and fragments within devices, potentially causing single event effects due to their short range. Thermal neutrons (below approximately 100 meV) and epi-thermal neutrons (below 1 MeV) may interact with devices through neutron capture by atomic nuclei. When a neutron is absorbed, the resulting excited nucleus is often unstable and subsequently undergoes radioactive decay. In cases where alpha particle decay occurs, the alpha particle can deposit ionization charge in a sensitive region, leading to an upset or other errors. The presence of isotopes such as boron-10, which have a high neutron capture cross section, significantly enhances this effect.

Borophosphosilicate glass (BPSG) was historically used as an isolation material between metal interconnect layers in devices. However, devices using BPSG showed high rates of soft errors in terrestrial applications due to neutron capture from cosmic ray showers in the atmosphere. Consequently, the use of BPSG diminished for this reason. Nevertheless, boron is now making a resurgence as a passivation agent in the fabrication of various types of integrated circuits, particularly in applications involving through-layer vias and other interconnects.

FUTURE TRENDS AND CONCERNS

Advancements in technology have led to scaling devices down to increasingly smaller feature sizes, which can impact various radiation effects differently. Devices with smaller features generally exhibit reduced susceptibility to total ionizing dose and displacement damage. This is because individual transistors have less volume available to trap charge and create lattice defects, resulting in minimal modification to device performance. However, the introduction of vertical structures like FinFETs at the 14nm node, while reducing gate thickness, increases total area and may start to reverse the trend of reduced cumulative radiation effects with smaller features.

Conversely, non-radiation concerns may intensify with smaller features. Thinner gates experience higher leakage currents, and the heightened electric fields in smaller devices contribute stress and decrease reliability.

Regarding single event effects, the impact of scaling is mixed. Smaller feature sizes mean smaller targets, leading to declining per-bit error rates in memory devices. However, manufacturers can pack more bits into the same area, maintaining relatively constant per-device error rates. Multiple-bit upsets, where one ion disrupts multiple cells, are becoming more prevalent with smaller technology nodes. This increase is due to multiple cells often fitting within the charge radius of a single ion track, posing challenges to traditional error detection and correction schemes. Moreover, smaller critical charge thresholds and lower bias voltages enhance the susceptibility of devices to ion-induced effects. Additionally, higher clock frequencies increase the likelihood of transients causing digital errors, as previously mentioned.

Figure 10 illustrates a growing concern regarding proton direct ionization (data adapted from [10] with added LET curve). Traditionally, most devices, with optical couplers being a notable exception, were thought to be too lightly ionized by protons to cause errors independently. However, starting around the 90nm technology node, evidence began to emerge that this general rule was breaking down, particularly in devices with a low critical charge.

When protons decelerate near stopping, their ionization energy deposition sharply increases, a phenomenon known as the "Bragg peak." This characteristic is common to all ions and forms the basis of proton cancer treatments, where energy is concentrated at a tumor site with minimal damage to surrounding tissue. In Figure 10, the upset rates for 65nm and 90nm SRAM devices rise almost in tandem with increased charge deposition at lower proton energies. This provides direct evidence that protons are affecting devices through direct ionization.

The concern centers on devices operating in environments abundant with protons, such as low Earth orbit or certain accelerator facilities. As long as devices only respond to indirect ionization, the low probability of a single proton undergoing a nuclear interaction within the device helps maintain manageable error rates. However, if all protons in such environments have the potential to directly induce errors, error rates could increase significantly.

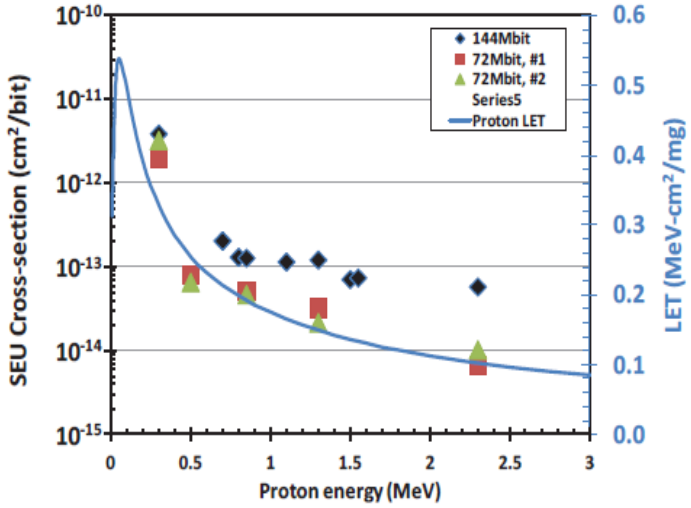

Figure 10: Proton-induced upset rates in 90nm and 65nm SRAM memories as a function of proton energy (data replotted from[10]). The curve shows the Bragg peak in the energy deposition curve for protons. It is clear that protons can upset the devicethrough direct ionization.

MITIGATION STRATEGIES

There are various techniques employed by part and circuit designers to mitigate the effects of radiation on microelectronics. Mitigation strategies for total ionizing dose typically begin at the process and component levels. The use of wide-bandgap materials such as SiC and GaAs can reduce charge trapping and offer additional benefits like high speed. Radiation hardness-by-design (RHBD) techniques [11] involve gate topologies that fully enclose the drain, trench isolation to replace field oxides prone to charge trapping, and meticulous design of gate and field oxide edges to minimize leakage paths.

Mitigation of single event effects can occur at multiple levels, from the process and component levels to the circuit and board levels. Latchup can be mitigated by incorporating an epitaxial layer that isolates charge wells under each node from the substrate, thereby disrupting parasitic transistors. Memory cells and latches can be made more resilient to upsets through advanced cell topologies. For instance, Figure 11 illustrates the topology of a dual-interlocked storage cell (DICE) memory element, where both nodes must be upset simultaneously to alter the logic state—making such an event highly improbable. However, a single particle at a steep angle striking both sensitive nodes could potentially defeat the cell. Figure 12 shows an example of triple-module redundancy (TMR) used to safeguard latch data, where the latch is replicated three times and a majority voter ensures the output remains unaffected by any single latch error. Some TMR implementations incorporate feedback to utilize the voted output for error correction, restoring full functionality to affected stages.

Each of these mitigation strategies incurs penalties in terms of area, power, or speed, which can deter their adoption by part manufacturers.

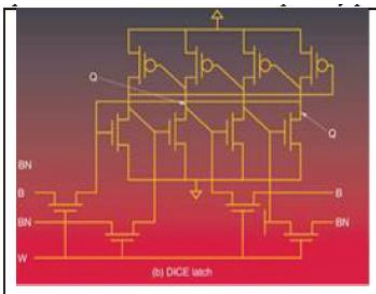

Figure 11: Topology of a dual-interlocked storage cell (DICE). Two separate nodes must be upset to reverse the logic state of the cell.

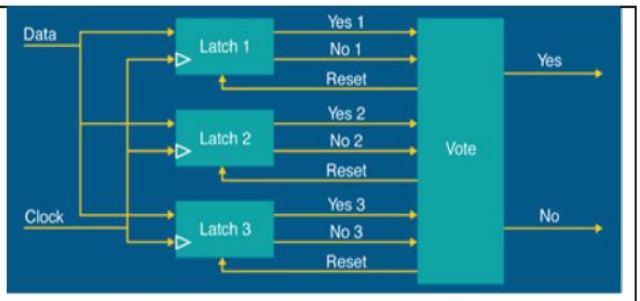

Figure 12: Example of triple-module redundancy (TMR) employed to protect a data latch. The latch is triplicated and the outputs voted. Any single latch in error will not affect the final result.

SUMMARY

Radiation effects in microelectronics are typically categorized into cumulative effects such as total ionizing dose and displacement damage, and single-event effects (SEE) caused by individual particles. SEE can either be destructive or non-destructive, often induced by heavy ions through direct ionization, and by protons and neutrons through nuclear collisions. Thermal neutrons can also be captured by nuclei, releasing alpha particles into sensitive device regions. Despite various mitigation strategies available, each introduces trade-offs in terms of power consumption, area, and speed, and none offer a universal solution. Challenges persist as technology advances towards smaller feature sizes.

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