Vol 4 Issue 5 June 2014

ISSN No : 2230-7850

International Multidisciplinary Research Journal

Indian Streams Research Journal

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RNI MAHMUL/2011/38595 **ISSN No.2230-7850**

Indian Streams Research Journal is a multidisciplinary research journal, published monthly in English, Hindi & Marathi Language. All research papers submitted to the journal will be double - blind peer reviewed referred by members of the editorial board.Readers will include investigator in universities, research institutes government and industry with research interest in the general subjects.

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Indian Streams Research Journal
ISSN 2230-7850
Volume-4 | Issue-5 | June-2014
Available online at www.isrj.net

FPGA IMPLEMENTATION OF PIPELINED STEERABLE GAUSSIAN SMOOTHING FILTER

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Abstract:-Smoothing filters have wide area of applications such as image and video analysis, which extends to Edge detection, motion analysis, line parameter estimation, and texture analysis. This can be achieved using directional smoothers. Directional smoothing filters which can achieve orientation in any arbitrary direction are essential. It is essential to have computing resources. Hardware devices having capability of parallel processing can be used to obtain real time performance. This is the property of steerability, in which several filtering operations outputs are linearly combined to achieve output of a directional filter which is arbitrarily oriented. Though the literature describes the several efficient FPGA implementations of the convolution operation for non-separable and separable, limited work is available related to steerable filter implementations. In this system, steerable Gaussian smoothing filters are implemented on an FPGA platform using Virtex-V evaluation board. The key advantages of FPGAs over DSP implementations include integration, performance and customization using design techniques of parallel and pipeline operations. A pipelined approach of convolution gives the less number of resources.

Keywords: Steerability, Directional filter, Virtex-V, Gaussian Filters, Parallel Processing, Pipelined Approach,

INTRODUCTION

Smoothing is achieved by convolution of an original image with an appropriate mask, such as a Gaussian mask. Image processing algorithms are mostly local and two dimensional (2-D). The output is computed using an N×N neighborhood of pixels of the input image around every pixel of interest, hence the result is obtained by means of a 2-D convolution As directional or orientation filters [7] are widely used in computer vision and image processing applications its response at any arbitrary position and orientation is obtained by tunning the filter to all possible positions and orientations. However, such an approach requires a large number of computations, and is thus not easily implementable in real time.

More effectively it is done by designing a family of basis filters, with the intension that a filter tuned at an arbitrary position or orientation can be expressed as a linear combination of these basis filters. Therefore, the output of the filter can be expressed as a weighted sum of the basis filter outputs. Filters having this property are called steerable filters.

For instance, a reduction in the number of multipliers can be achieved through the use of separable filters. A separable filter of size N × N can be expressed as the convolution between two filters of sizes N × 1 and 1 × N, respectively. Gaussian filters oriented at 0^0 or 90^0 are separable.

LITERATURE SURVEY

In this paper, a Gaussian steerable multidirectional filter bank implementation on FPGA is proposed. Literature gives the efficient implementations of separable and non-separable 2D convolution techniques but steerable filter implementation on FPGA has limited research. In [1], Area-Efficient 2-D shift-variant convolvers for FPGA-based digital image processing are proposed. They proposed several novel FPGA-efficient architectures for generating a moving window over a row-wise print path, and provided a criteria to choose the optimum one for any design point. Hui Zhang et. al. proposed a Multiwindow Partial Buffering Scheme for FPGA Based 2-D Convolvers [2]. Erke Shang et. al. in [3] puts forth about Architectures for Generalized 2D FIR Filtering using Separable Filter Structures. The problem of generalized 2D FIR filtering for large filter kernel sizes can be computationally prohibitive when required in real-time In [4], C.S Bouganis et. al. emphasized on steerable

pyramid wavelet construction for image decomposition and feature detection, and its implementation on FPGA. Erke Shang et.al. used steerable filters for lane detection and implemented it on FPGA [5]. If the approach presented in [4] and [5] are used then large number of basis filters would be required. Instead, regardless of the desired angular resolution, Gaussian smoothers can be steered via the application of three 1D filtering operations [7].

A. Convolution

Convolution which is a common image processing operation and is can be given as sum of products among the input image and a smaller image like array called the convolution Kernel. Using convolution, several imaging operations can be achieved depending on the selection of values in the convolution kernel.

$$H(m,n) = \sum_{i=0}^{height-1} \sum_{j=0}^{width-1} g(i,j) f(m-i, n-j) \qquad (1)$$

Where f denotes the input image, h is the output g is the filter image.

B. Gaussian Mask

1D Gaussian distribution has the following form[1]:

$$g(x,y) = \frac{1}{\sqrt{2\pi\sigma^2}} e^{-x^2/2\sigma^2} \qquad (2)$$

In 2D, a circularly symmetric Gaussian has the form [1]

$$g(x,y) = \frac{1}{2\pi\sigma^2} e^{-(x^2+y^2)/2\sigma^2} \qquad (3)$$

where g is the weight of Gaussian kernel at the location with coordinates x and y. The σ parameter is the standard deviation of the Gaussian distribution .The term $\frac{1}{2\pi\sigma^2}$ is normalization constant.

An important application of separability is that convolution with a 2D Gaussian kernel can be replaced by a cascade of 1D Gaussian kernels, makes the whole convolution process much more efficient by using fewer number of multiplications [5]. Hence convolution using separable filter is performed in two steps. The input is convolved with a filter of size N×1, while the result is convolved with a filter of size 1×N [5]. Hence in this case of separable convolution, a total of 2N multiplications and 2N- 2 additions are required which is significantly less compared to the non-separable case, specifically for large-scale filters.

C. Steerable and Separable Filters

Steerability implies that the output of a filtering operation, $O_\theta(x,y)$ using a filter oriented at an angle θ can be computed as the linear combination of a finite set of M outputs { $O\theta_0(x,y)$, $O\theta_1(x,y)$, ……..,$O\theta_{M-1}(x,y)$ } obtained by applying the same filter oriented at directions $\theta_0, \theta_1, \ldots\ldots\ldots\ldots, \theta_{M-1}$ respectively. A 2D separable and steerable filter can be written as [5]:

$$g\theta(x,y) = \sum_{r=-R}^{R} g_{iso}(x - r\cos(\theta), y - r\sin(\theta)) g^{1D}(r) \qquad (4)$$

where it was assumed that the size of $g^{1D}(r)$ is equal to 2R+1.

The filter described in (4) can be applied to an image I (x, y) in two steps. In the first step, the filter ? iso(? , ?) is applied to the image.

$$I\text{iso}(x,y) = I(x,y) * g\text{iso}(x,y) \qquad (5)$$

In the second step, the following operation is applied to the image I iso (x, y)

$$I_\theta(x,y) = \sum_{r=-R}^{R} I_{iso}(x - r\cos(\theta), y - r\sin(\theta)) g^{1D}(r) \qquad (6)$$

The operation described in (5) and (6) is equivalent to the operation where Gaussian directional smoothing filter

(DSF) oriented at direction ? filters the input image I(x, y).

PROPOSED SYSTEM

A. Steerable FPGA Implementation

In [7], a Gaussian steerable multidirectional filter bank consisting of M directional 2D Gaussian smoothers is implemented by decomposing each of the M smoothers in three 1D Gaussian filters. The first two 1D filters are employed horizontally and vertically, while the third 1D filter is applied in the direction of interest.

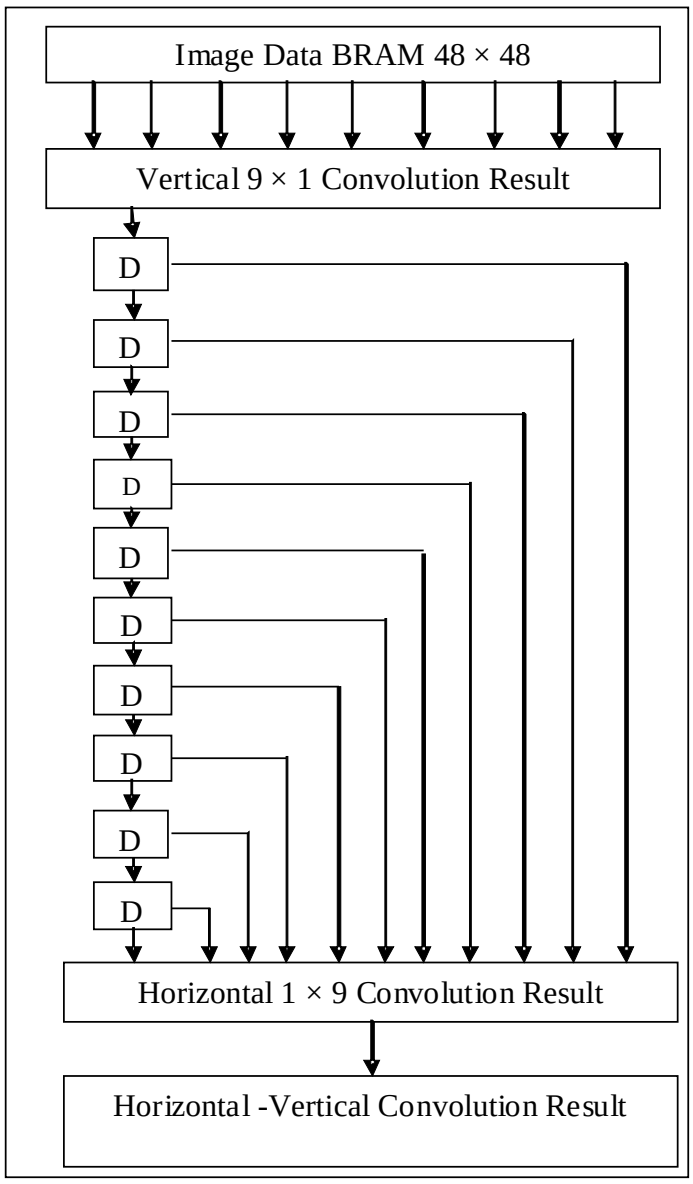

Fig.1: Block Diagram Representation of Pipelined Convolution

The first two 1D filters are essentially equivalent to a 2D separable Gaussian filter, and they are independent of the filter orientation. As a result, they are applied only once, and they do not significantly affect the resource utilization, regardless of the number of filter orientations, M, used in the filter bank. The third 1D filter needs to be employed M times. Nevertheless, some initial smoothing has already been applied to the image owing to the first two 1D filters. As a result, a down sampling factor can be introduced to reduce the number of operations. Therefore, the resource requirements are sufficiently low so that pipelining techniques can be used for a real-time implementation. The block diagram of this convolution operation is shown in Fig.1.

BRAM is used to store a test image using .coe file. After 9 × 1 vertical convolution, the operation is performed so that after 9 clocks a horizontal convolution operation is possible. The vertical convolution results are delayed. Hence simultaneous vertical and horizontal convolution operation is possible. A pipelining technique can be used to obtain higher throughput.

B. Steerable FPGA Implementation

The last stage of the Gaussian steerable approach uses an operation equivalent to 1D filtering at the direction of interest. This operation is applied to the smoothed image obtained by the previous stages, that have filtering of the original image using an isotropic Gaussian filter. This Gaussian mask can be rotated in different directions to obtain steerable output at different directions.

In the steerable concept, pixels are accessed in different directions depending on the decimation factor. Then, the pixels are multiplied with the weights of Gaussian mask and finally given to adder to obtain final steerable results in a particular directionThe final results obtained in each particular direction are our required steerable results. The block diagram representation of implementing steerable concept on the results of pipelined separable convolution in horizontal and vertical direction is shown in Fig.3.

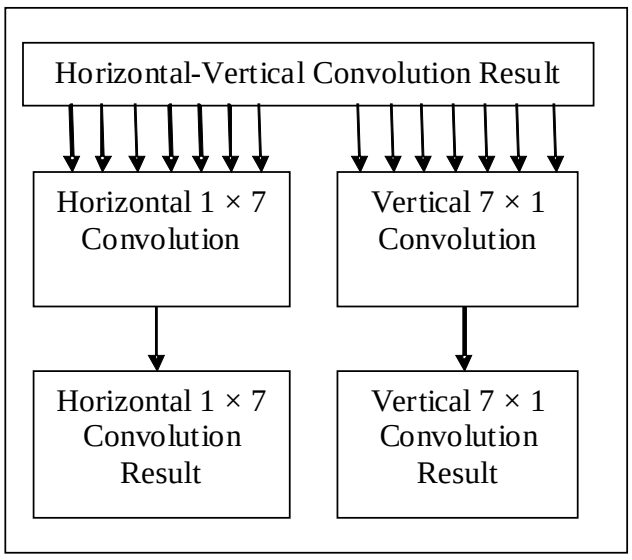

Fig.2: Block Diagram Representation of Steerable Implementation.

RESULTS AND DISCUSSION

Here, experiments are performed on image of size of 48 × 48 using Gaussian mask which is separable of size 9 × 9 to obtain the steerable filter results. Directional Gaussian Implementation of these filters is carried out using Xillinx ISE 13.4i and FPGA implementation on Virtex-5 board. The simulation results of convolution are shown in Fig. 3 and device utilization summary of the implementation is given in Table 1.

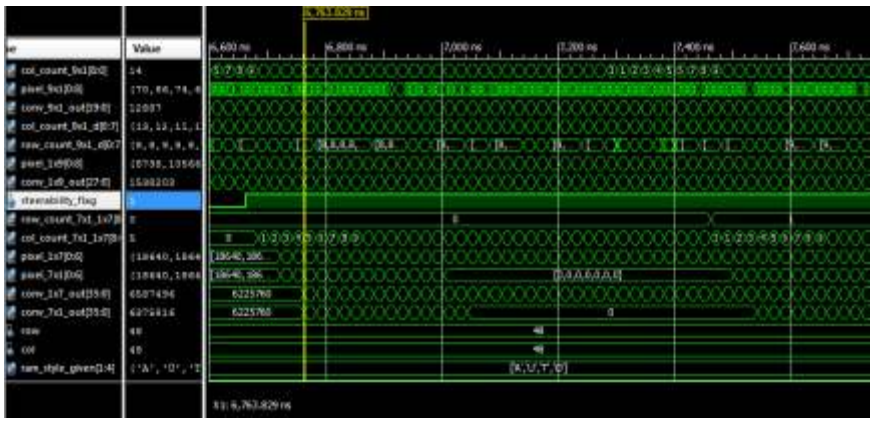

Fig. 3: Simulation Results of Convolution Operation

Table 1: Device Utilization Summary of Implementation

Device Utilization Summary (estimated values)			
Logic Utilization	**Used**	**Available**	**Utilization**
Number of Slice Registers	850	32640	2%
Number of Slice LUTs	762	32640	2%
Number of fully used LUT-FF pairs	334	1278	26%
Number of bonded IOBs	18	480	3%
Number of Block RAM/FIFO	5	132	3%
Number of BUFG/BUFGCTRLs	2	32	6%
Number of DSP48Es	15	288	5%

CONCLUSION AND FUTURE SCOPE

In this paper, an efficient steerable filter implementation on FPGA has been presented. However, it also employs a steerable implementation in which 2D filtering operations utilizing directional Gaussian smoothing filters, which are not separable in general, are replaced by an equivalent set of three 1D filtering operations. The first two operations are performed in a pipelined manner, in order to achieve high throughput. The third 1D filtering operation is employed consecutively to the first two operations in order to conserve memory resources. Pipelined approach is used to achieve high throughput. It will reduce the BRAM requirements and increase multiplier usage.

ACKNOWLEDGMENT

It is my pleasure to get this opportunity to thank my beloved and respected Guide Dr. S.K.Shah who imparted valuable basic knowledge of Electronics specifically related to VLSI. We are grateful to department of Elect. and Tele. Comm., Smt. Kashibai Navale College of Engineering, Pune for providing us infrastructure facilities and moral support.

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