Vol 6 Issue 5 June 2016

ISSN No : 2230-7850

International Multidisciplinary Research Journal

Indian Streams Research Journal

Welcome to ISRJ

RNI MAHMUL/2011/38595 **ISSN No.2230-7850**

Indian Streams Research Journal is a multidisciplinary research journal, published monthly in English, Hindi & Marathi Language. All research papers submitted to the journal will be double - blind peer reviewed referred by members of the editorial board.Readers will include investigator in universities, research institutes government and industry with research interest in the general subjects.

Address:-Ashok Yakkaldevi 258/34, Raviwar Peth, Solapur - 413 005 Maharashtra, India
Cell : 9595 359 435, Ph No: 02172372010 Email: ayisrj@yahoo.in Website: www.isrj.org

ISSN: 2230-7850 Impact Factor : 4.1625(UIF) Volume - 6 | Issue - 5 | June - 2016

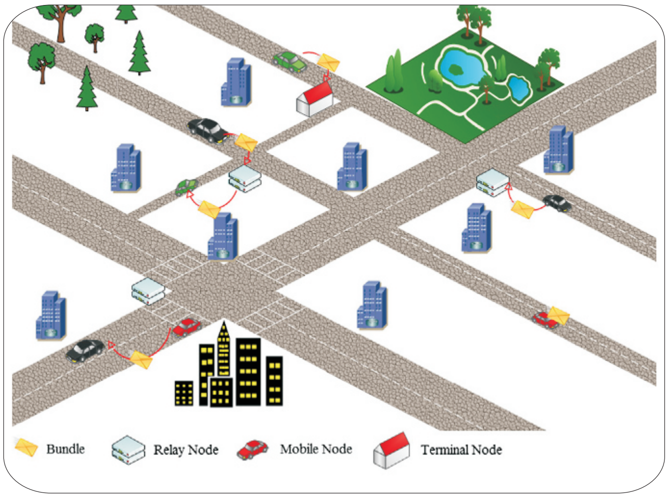
Indian Streams Research Journal

A COMPREHENSIVE SURVEY OF ROUTER FUNCTIONALITY

Ananth Kumar M. S.
Assistant Professor, ECE dept., BTLITM, Bangalore,

Co - Author Details :

Dr. D. Jayadevappa
Prof. & HOD, IT dept., JSSATE, Bangalore,



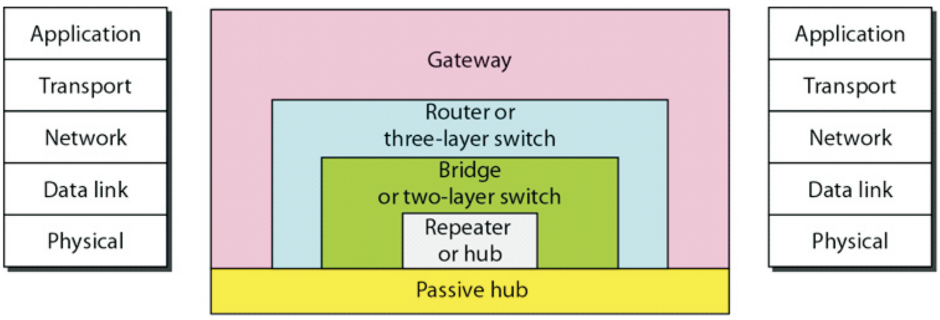
ABSTRACT

This work is in continuation with my previous Research & survey on Routers, its classification, history & evolution of various generations of Router architectures, popular Routing Algorithms etc. This technical paper surveys the Need for Routing, Router - its basics, Functionality, Data path & Control plane functions, Generic architecture, building blocks, various types of switch fabrics, concepts of shared bus, memories & cross point switching etc.

KEYWORDS :Routing, Switching, Switching Fabric, Shared Bus, Shared Memory, Cross Bar Data, Routing Processor.

Routing v/s Switching

Five categories of connecting devices [Fig.1]



Router – Definition

A router (including a wireless router) is a specialized networking device connected to two or more networks running software that allows the router to move data from one network to another. Router functions in an Internet protocol based network operate at the network layer (OSI Model's layer 3). The primary function of a router is to connect networks together and keep certain kinds of broadcast traffic under control. [3]

Router Basics[1]

Need for Router

- We need to move traffic from one part of the network to another
- Connect end-systems to switches, and switches to each other by links
- Data arriving to an input port of a switch have to be moved to one or more of the output ports

Internet: "network of networks"

- Any to any reach ability
- but loosely hierarchical
- Routing protocols populate routing tables in the routers

Traffic Aggregation

- Through multiplexing and switching
- Access Networks
- Edge
- Core

Router Functionality

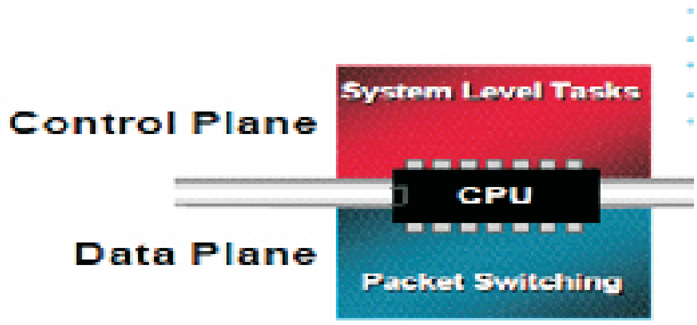
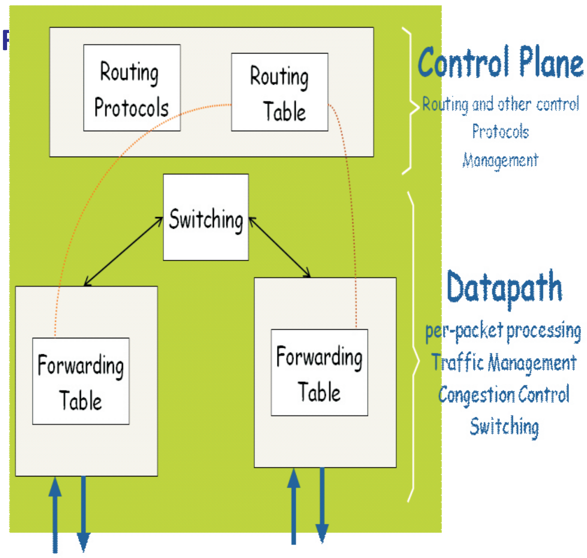


Fig.2 [5]



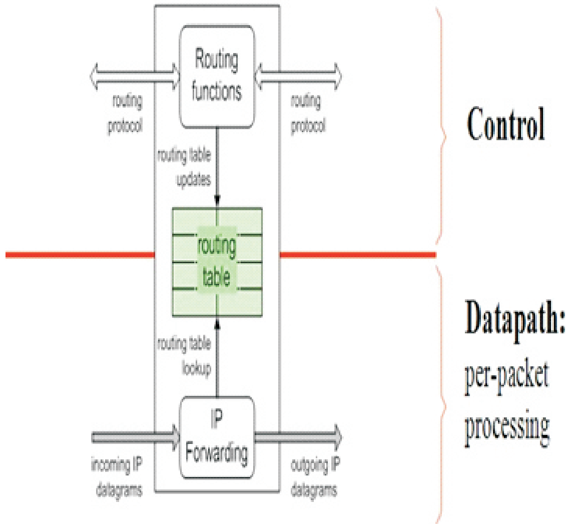


Fig.3 & 4

Basic Architectural Componentsof an IP Router

Router functions can also be divided as[6]

Datapath functions [refer Fig.2,3& 4]

o Functions applied to every packet.

E.g. header lookup, forwarding, scheduling.

o Handled by input, output port and switching fabric.

o Directing a data packet to an outgoing link –Individual router using a forwarding table

Control functions

o Functions not applied to every packet.

E.g. system configuration, management, table update.

Handled by routing processor

o Goal for high speed requires increase in the rate at which data path functions are performed.

o Computing paths the packets will follow –Routers talking amongst themselves –Individual router creating a forwarding table

Packet reception[4]

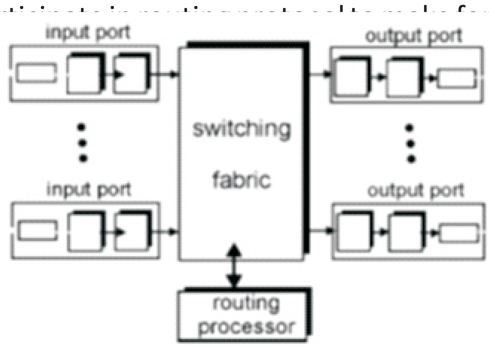
- Interface FIFO (ring buffer?) holds groups of bits as they arrive
- Packet queued until treated by central CPU or interface card
- CPU (throw interrupt)
- Check CRC, is there space in memory...
- Packet classification (Dropped? Accepted? Switching method?)
- Moved to input hold queue

Packet forwarding

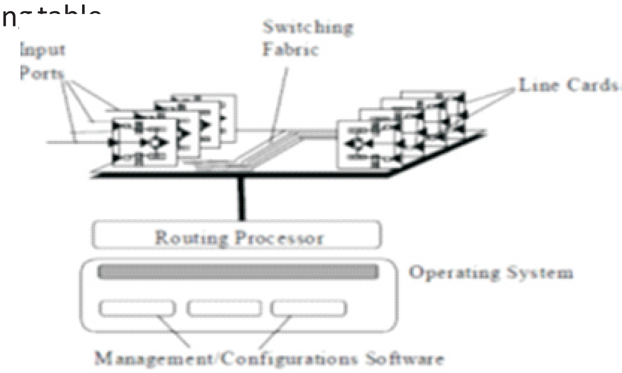
• Look up routing table
• Rewrite header (Ethernet, NAT?, TTL, checksum...)
• Packet moved to output hold queue
• **Forwarding: data plane**
o Directing a data packet to an outgoing link
o Individual router using a forwarding table
• **Routing: control plane**
o Computing paths the packets will follow
o Routers talking amongst themselves
o Individual router creating a forwarding table
• Decentralized switch using forwarding table in input port memory
• goal: complete input port processing at 'line speed'
• queuing: if datagrams arrive faster than forwarding rate into switch fabric

TWO KEY ROUTER FUNCTIONS:
- run routing algorithms/protocol (e.g. RIP, OSPF, BGP)
- forwarding datagrams from incoming to outgoing link

Classification of Routing Architectures – a Generic Router [Fig.4 & 5]
A generic router has four components: [2]
I. Input Ports
o Entry point for incoming packet.
II. Output Ports
o Exit point of the packet.
III. Switching Fabric
o Switch the packet from I/P port to O/P port.
IV. Routing Processor
o P[illegible]ardin[illegible]



A Generic Router Architecture



Architecture of a router

Fig.4 & 5

Input Port: An input port is the point of attachment for a physical link and is the point of entry for incoming packets. Ports are instantiated on line cards, which typically support 4, 8, or 16 ports [Fig.6].

An input port provides several functions:

1.It carries out data link layer encapsulation and decapsulation.

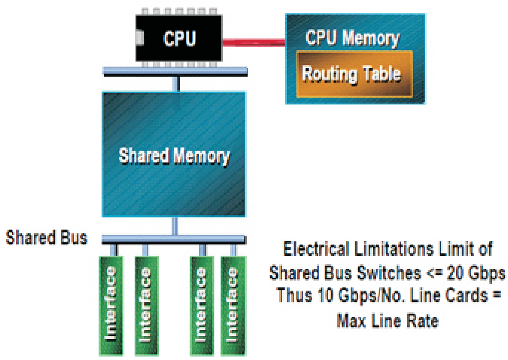
2.It may also have the intelligence to look up an incoming packet's destination address in its forwarding table to determine its destinationport (this is also called route lookup). The algorithm for route lookup can be implemented using custom hardware, or each line card may be equipped with a general-purposeprocessor or a specialized network processor. When equipped with a ASIC/processor, this unit is called as Forwarding Engine (FE).

3.In order to provide QoS guarantees, a port may need to classify packets into predefined service classes.

4.A port may need to run datalink-level protocols such as SLIP and PPP, or network-level protocols such as PPTP. Once the route lookup is done the packet needs to be sent to the outputport using the switching fabric.

SWITCHING FABRIC:

The switching fabric interconnects input ports with output ports. A router is classified as input-queued or output queued depending on the relative speed of the input ports and the switching fabric. If the switching fabric has a bandwidth greater than the sum of the bandwidths of the input ports, then packets are queued only at the outputs, and the router is called an output-queued router. Otherwise, queue[illegible] s cal[illegible]



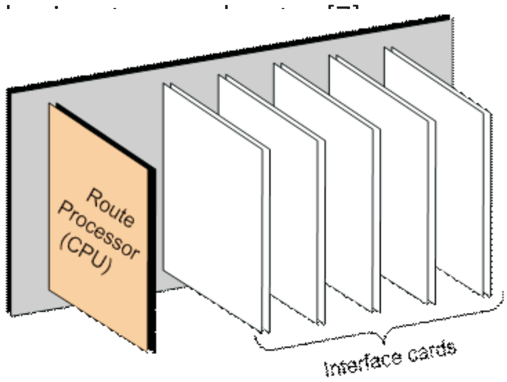
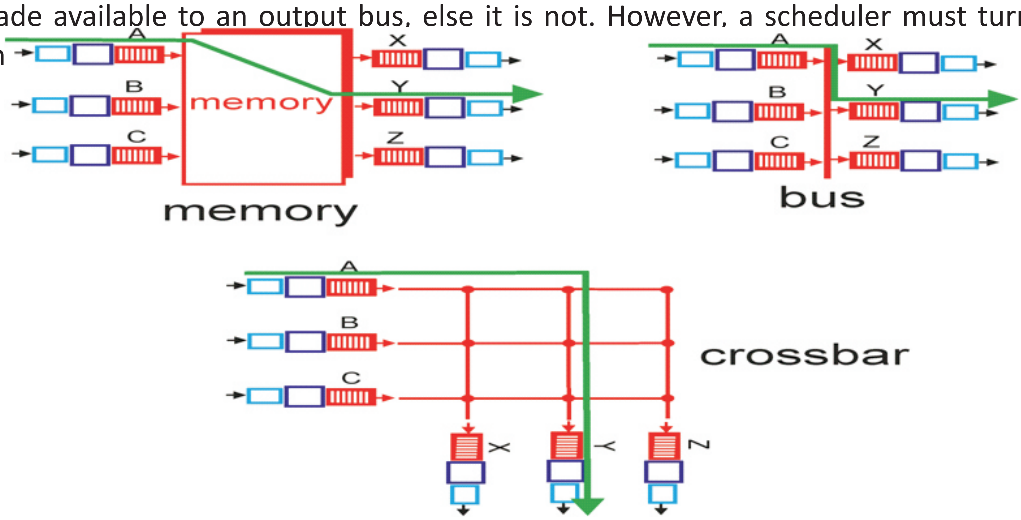


Fig.7

Fig.12

The switching fabric can be implemented using many different techniques. The most common switch fabric technologies in use today are busses, crossbars, and shared memories. The simplest switch fabric is a bus that links all the input and output ports. However, this is limited in capacity by the capacitance of the bus and the arbitration overhead for sharing this single critical resource. [Fig.7& 9]

Unlike a bus, a crossbar provides multiple simultaneous data paths through the fabric. A crossbar can be thought of as 2N busses linked by N*N crosspoints: if a crosspoint is on, data on an input bus is made available to an output bus, else it is not. However, a scheduler must turn on and off crosspoin



• Bus
o Limit due to Arbitration overheard and capacitance.
• Crossbar
o A scheduler turns on and off the cross-points.
• Shared Memory
o Only pointers to packets are switched. Limited by the memory access time.

Thus, the scheduler limits the speed of a crossbar fabric. In a shared-memory router, incoming packets are stored in a shared memory and only pointers to packets are switched. This increases switching capacity. However, the speed of the switch is limited to the speed at which we can access memory.

Unfortunately, unlike memory size, which doubles every 18 months, memory access times decline only around 5% every year. This is an intrinsic limitation with shared-memory switch fabrics.

Shared Bus

The simplest switch fabric is a bus that links all the input and output ports. However, this is limited in capacity by the capacitance of the bus and the arbitration overhead for sharing this single critical resource.
• Transfer data from input to output, ignoring scheduling and buffering
• Usually consist of links and switching elements
• Simplest switch fabric
• think of it as 2N buses in parallel
• Used here for packet routing: cross-point is left open long enough to transfer a packet from an input to an output
• For fixed-size packets and known arrival pattern, can compute schedule in advance (e.g., circuit switching)

• Otherwise, need to compute a schedule on-the-fly (what does the schedule depend on?)

Sw

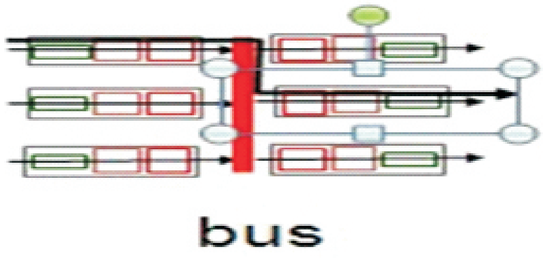


Fig.9

• datagram from input port memory
• to output port memory via a shared bus
• bus contention: switching speed limited by bus bandwidth
• 1 Gbps bus, Cisco 1900: sufficient speed for access and enterprise routers (not regional or backbone)
• Port mapping intelligence in line cards (processor based)
• Ring or Bus based backplane to connect line cards
• Bottleneck -> performance impact (discuss bus and ring)
• Lookup cache on line cards (for better performance)
• For switch, cross connect table (port mapping entries) only changed when calls are setup / torn down
• For datagram router, ask the control processor if the entry is not found in local forwarding table or automatically updated.

Shared Memory

• Route only the header to output port
• Bottleneck is time taken to read and write multiported memory
• Doesn't scale to large switches
• But can forn

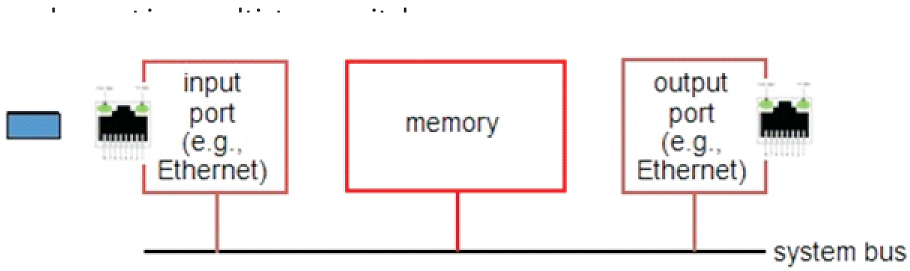


Fig.10

Switching Via Memory[1]

• A computer with multiple line cards
• Processor periodically polls inputs (or is interrupted)
• Most Ethernet switches and cheap packet routers

• Bottleneck can be CPU, host-adaptor or I/O bus, depending on the traffic scenario
• Line card can be cheap (no CPUs on line cards!!)
Switching Via an Interconnection Network
• overcome bus bandwidth limitations
• Banyan networks, other interconnection nets initially developed to connect processors in multiprocessor
• Advanced design: fragmenting datagram into fixed length cells, switch cells through the fabric.
o Segmentation and Reassembly (SAR)
Discuss overheads
• Cisco 12000: switches Gbps through the interconnection network
• Bottleneck in second generation switch is the bus (or ring)
• Third generation switch provides parallel paths using a switch fabric
• self-routing fabric
• output buffer is a point of contention
• unless we arbitrate access to fabric
• potential for unlimited

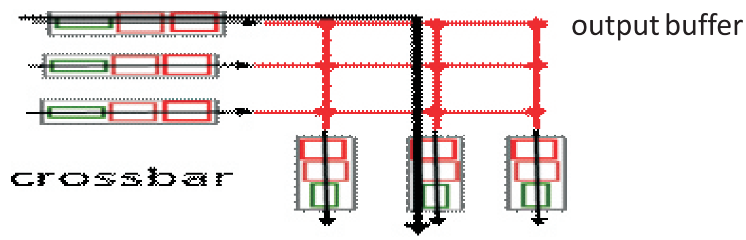


Fig.11

Cross Bar Data

• Simplest switch fabric
o think of it as 2N buses in parallel
• Used here for packet routing: cross-point is left open long enough to transfer a packet from an input to an output
• For fixed-size packets and known arrival pattern, can compute schedule in advance (e.g., circuit switching)
• Otherwise, need to compute a schedule on-the-fly (what does the schedule depend on?)
• Simplest switch fabric
• think of it as 2N buses in parallel
• Used here for packet routing: cross-point is left open long enough to transfer a packet from an input to an output
• For fixed-size packets and known arrival pattern, can compute schedule in advance (e.g., circuit switching)
• Otherwise, need to compute a schedule on-the-fly (what does the schedule depend on?)
• N input ports, N output ports
– One per line card, usually
• Every line card has its own forwarding table/classifier/etc --- removes CPU bottleneck

Output Port: [2]

Output ports store packets before they are transmitted on the output link. They can implement sophisticated scheduling algorithms to support priorities and guarantees. Like input ports, output ports also need to support datalink layer encapsulation and decapsulation, and a variety of higher-level protocols

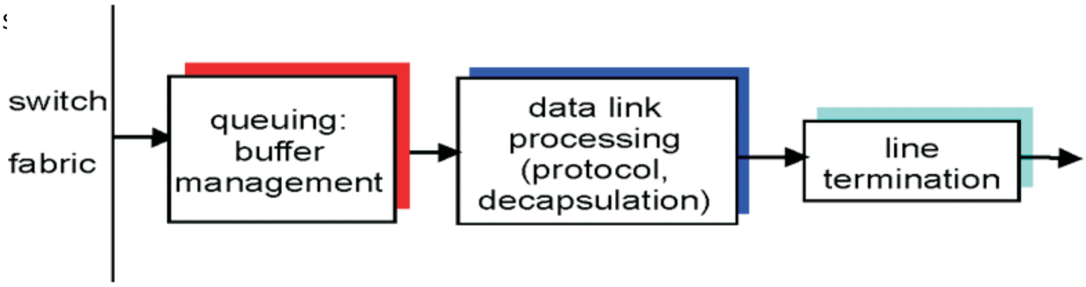


Fig.12

An output port stores packets and schedules them for service on an output link.

Output ports store packets before they are transmitted on the output link. They can implement sophisticated scheduling algorithms to support priorities and guarantees. Like input ports, output ports also need to support datalink layer encapsulation and decapsulation, and a variety of higher-level protocols.

An output port stores packets and schedules them for service on an output link.

- Buffering required when datagrams arrive from fabric faster than the transmission rate
- Scheduling discipline chooses among queued datagrams for transmission
- Packets heading for same output link need to be stored in a buffer; so as to avoid packet loss.
- Supports sophisticated scheduling algorithms to support priorities and guarantees.
- Support data link layer functionality

ROUTING PROCESSOR:

The routing processor computes the forwarding table, implements routing protocol, and runs the software to configure and manage the router. It also handles any packet whose destination address cannot be found in the forwarding table in the line card. [2]

The routing processor participates in routing protocols and creates a forwarding table that is used in packet forwarding.

It computes the forwarding table based on the updates received from other routers according to routing protocol. Also runs the software to configure and manage the router.[Fig.12].

CONCLUSION:

We all are aware that Routers are very popular in the Networks & Internet applications for Data communications between different Communications equipment, Computers, Smart phones etc. Routing is a complex function that can be accomplished in 2 ways by using - Popular Routing Algorithms as I mentioned in my previous survey paper&Popular Routing Architectures as I continue my Survey towards arriving at my Innovative next generation Router Architecture.

REFERENCES

[1] webhome.csc.uvic.ca/~wkui/Courses/CSC467/4-SwitchingArch.ppt
[2] Network Router Architecture: A survey SanjeevKayath Prof. AshfaqKhokhar skayath@eecs.uic.edu EECS, University of Illinois, Chicago
[3]http://www.inetdaemon.com/tutorials/internet/ip/routing/define_router.shtml
[4] http://lig-membres.imag.fr/heusse/archi_routeur.pdf
[5]www.cisco.com/networkers/nw99_pres/601.pdf
[6] www.ece.uic.edu/~skayath/569/Router.ppt
[7] https://www.cs.cornell.edu/skeshav/papers/routertrends.pdf
[8] International Journal of Scientific & Engineering Research, Volume 4, Issue 5, May-2013 706 ISSN 2229-5518 IJSER © 2013 http://www.ijser.org A Study of Advanced Switching Fabric Design of a “Router” AlokSahu* Dr. Bharat Mishra* Gauri Shankar Kushwaha
[9] http://www.cs.ccsu.edu/~stan/classes/CS490/Slides/Networks4-Ch4-2.pdf