Research Papers

A STUDY ON THE RADIATED SUSCEPTIBILITY OF PRINTED CIRCUIT BOARDS AND THE EFFECTS OF VIA FENCING

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ABSTRACT:-

Given the growing likelihood of modern electronic systems being exposed to high intensity radiated fields (HIRF) environments, there is increasing interest in understanding how these environments affect electronic systems. Backdoor coupling, in particular, is a significant concern for all electronics, yet the mechanisms behind it remain poorly understood. This study focuses on printed circuit board (PCB) backdoor coupling and the impact of via fencing. Previous research, which mainly examines ideal stackups, suggests that via fencing significantly reduces edge radiation. Our study employs both full wave electromagnetic modeling and experimental verification to investigate both ideal and practical PCB stackups. In the ideal scenario, our findings align with prior research, showing that via fencing substantially reduces coupling. However, in the practical scenario, we account for component footprints and traces that naturally create openings in the top ground plane. Both simulation and experimental data reveal that via fencing in this practical setup does not significantly mitigate coupling. This suggests that PCB edge coupling is not the dominant coupling mechanism, even when considering varying angles of incidence and polarization.

KEYWORDS : backdoor coupling; full wave modeling; high intensity radiated fields (HIRF); induced voltage; parallel plate resonance; printed circuit board (PCB) coupling; radiated susceptibility; viafencing; via stitching

1. INTRODUCTION

In recent years, there has been increasing concern about the impact of high intensity radiated fields (HIRF) environments on electronic devices and systems. These fields are generated by various sources, including high-power long-range communication antennas and directed energy weapons, often referred to as intentional electromagnetic interference (IEMI) sources. This concern extends to both civilian and military applications. Consequently, the Federal Aviation Administration (FAA) and the Department of Defense (DoD) have implemented hardening requirements and are working to better understand the effects of HIRF environments on electronic devices【1–8】. According to these standards and other reports, typical field strengths in HIRF environments can reach tens of kilovolts per meter (10

kV/m)【9–11】. As demonstrated in our results, such field strengths can easily induce voltages of 10 V or more, which is alarming for modern electronics that typically operate at supply voltages of 5 V or 3.3 V. Moreover, the trend towards lower supply voltages to meet power and thermal requirements exacerbates this issue.

Due to the complexity of modern electronic systems, this issue has been studied at various subsystem levels, ranging from components【9,12–14】and printed circuit boards (PCBs)【15–20】to cables【21–27】and enclosures【15,25–30】, with some research even considering entire systems【31】. The problem is typically divided into four areas of study: coupling, energy distribution, device response, and system response.

This work specifically focuses on the coupling area, which is generally divided into two primary categories: front door coupling and backdoor coupling. Front door coupling refers to coupling to intentional antennas, while backdoor coupling involves coupling to unintentional antennas, such as wires, cables, PCB traces and planes, and component bondwires. The aim of this study is to enhance the understanding of the mechanisms behind backdoor coupling at the PCB level and to identify the key parameters that affect the degree of coupling. This knowledge could lead to the development of mitigation techniques that reduce coupling in HIRF environments, thereby decreasing the risk of system interruption or damage.

This study provides insights into PCB power and ground plane coupling and the effects of via fencing. To our knowledge, there has been limited investigation into PCB coupling in general, with related work primarily focusing on PCB emissions. Although emissions studies are complementary to radiated susceptibility studies due to the principle of reciprocity, it is important to avoid directly applying conclusions from one domain to the other.

Before discussing the existing literature on this topic, it is important to clarify terminology to prevent confusion. In this paper, the term “via stitching” refers to vias placed throughout the inner area of a PCB, while “via fencing” refers to vias placed around the perimeter of a PCB. Sparse via stitching naturally occurs in multilayer PCBs when grounding various component pads, but in some cases, additional via stitching is implemented to maintain low ground plane impedance and shorten return paths【32】. It is also worth noting that the term “via shielding” sometimes refers to surrounding specific traces with grounding vias to reduce crosstalk【33–35】.

The existing literature includes substantial research on reducing PCB emissions using various techniques. For instance, the 20H rule, a commonly referenced guideline, suggests pulling the power plane back from the PCB edge by twenty times the dielectric thickness【36–45】. There is significant debate over the effectiveness of this method, indicating that its success may depend on other factors, such as the PCB stackup. Other studies have investigated via fencing around the PCB perimeter to create a pseudo Faraday cage【36,38,46–51】. Additionally, some groups have explored advanced techniques such as edge plating【36,38】and the incorporation of electromagnetic bandgap structures【52】.

Many existing studies focus on emissions and often base their results on ideal PCB stackups【36–38,46,47,50,51,53】. These ideal stackups do not consider the presence of traces and vias that cause discontinuous planes. While such approaches have value, their conclusions may not necessarily apply to practical stackups and layouts.

This work makes two key contributions. First, it provides a novel investigation into the radiated susceptibility of PCBs and the effects of via fencing. Second, it offers a comparison between ideal and practical PCB stackups, which has not been addressed in the prior work cited

here. This comparison is crucial as it sheds light on whether via fencing significantly mitigates coupling in realistic scenarios.

This work is organized as follows: Section 2 discusses the theory behind power plane resonance and traditional via fencing approaches. Section 3 details the modeling and experimental methods used in this study. Section 4 presents a combination of simulated and experimental data for both an ideal multilayer PCB and a practical multilayer PCB. Finally, Section 5 offers a further discussion of the results and outlines plans for future work.

2. THEORY

2.1.Plane Coupling Theory

When a plane wave is incident on a PCB, it excites resonant modes on the planes and traces, depending on the PCB's geometry and dielectric material. Specifically, the PCB power and ground planes form a dielectric-loaded cavity or a parallel plate waveguide【15,23,30,36,54–5. The resonant frequencies (f_{mn}) of an ideal parallel plate waveguide can be calculated by considering the transverse magnetic (TM_{mn}) modes as follows:

$$f_{mn} = \frac{c}{2\sqrt{\varepsilon r}}\sqrt{\left(\frac{m}{a}\right)+\left(\frac{n}{b}\right)} \quad (1)$$

In this context, m and n are the mode indices, c is the speed of light, ϵr is the relative permittivity of the substrate, a and b are the length and width of the plates, respectively. For a 3D rectangular cavity, this equation would typically include a third term related to the height of the cavity. However, in practical PCBs, the vertical distance between the planes is much smaller than the wavelengths of interest, allowing us to ignore such modes. It should be noted that this equation applies to ideal parallel plates and does not directly extend to the multi-layer PCB structures studied here. For multi-layered structures and non-rectangular PCBs, eigenvalue analysis is generally used to determine resonant modes【23】.

As an example, Figure 1 illustrates the electric field pattern for multiple resonant frequencies, including the fundamental TM10 and TM01 modes, as well as higher-order modes that can be excited in an ideal PCB structure. The electric field intensity varies across the power plane, resulting in variations in the measured induced voltage. Notably, at the nodes of the standing wave patterns (blue regions in the plots), the induced voltage is minimal.

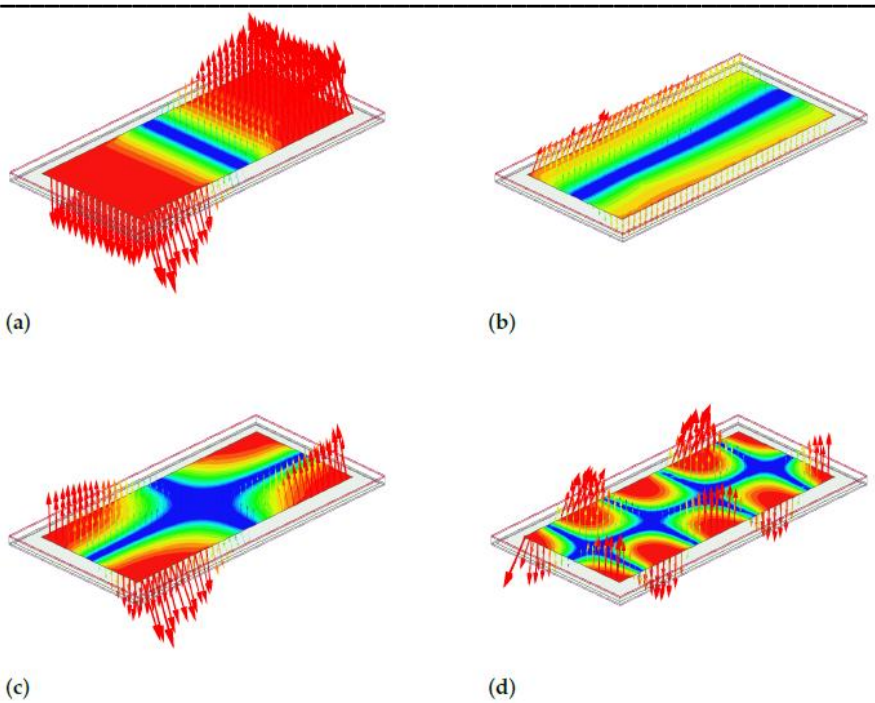

Figure 1. Electric field patterns for a sample of transverse magnetic (TM) resonant modes within afour-layer printed circuit board (PCB): (**a**) TM_{10}, (**b**) TM_{01}, (**c**) TM_{11}, and (**d**) TM_{41}.

2.2.Via Fencing Theory

Most modern PCBs have at least four layers, typically including external signal layers and internal power and ground planes. Components are usually placed on both sides of the board to reduce size and maximize layout efficiency, necessitating the use of signal vias to transition signals between layers.

Leveraging the principle of reciprocity, it is useful to first consider this scenario from an emissions perspective. As current travels through these signal vias, radially propagating waves are generated within the power and ground planes, which effectively function as a parallel plate waveguide【36,37,49】. When these waves reach the board's perimeter, some energy is reflected due to impedance mismatch, while some is radiated away from the board.

Existing literature suggests that via fencing and perimeter plating increase reflections within the PCB, thereby reducing radiation. Consequently, via fencing and other edge treatment techniques might also mitigate coupling to the power and ground planes from an external plane wave. This work directly addresses this question.

3. MATERIALS AND METHODS

Both modeling and experimental procedures were employed to investigate the effectiveness of via fencing in reducing coupling to the PCB planes. All tested PCBs were designed identically, except for variations in via fencing density along the perimeter. A single surface mount sub-miniature version A (SMA) connector was used to measure the power plane voltage in a controlled manner. To ensure the simulation closely matched the experimental setup, the SMA connector was also included in the model.

3.1.Full Wave Modeling

Each design in this study underwent simulation using Ansys High Frequency Structure Simulator (HFSS), a full-wave electromagnetic simulation application. The PCB designs were excited with a plane wave having a 1 V/m electric field strength. It is important to note that the choice of 1 V/m for the field strength in this study was for convenience, resulting in induced voltages that were relatively low, typically in the millivolt range in the worst case scenario. However, when scaled to match typical field strengths encountered in HIRF environments, these voltages can escalate to levels capable of causing disruption and potentially permanent damage, as discussed previously.

A perfectly matched layer (PML) boundary condition was applied to replicate free space conditions, and a lumped port with a 50 Ω impedance was used as the load. In the ideal stackup, the port was positioned between the inner power and ground planes, whereas in the practical stackup, the port was situated at the end of an SMA connector (refer to Section 4 for model diagrams). Each model underwent frequency domain simulation across a frequency range of 0.1 to 10 GHz.

To measure the induced voltage at the port, a line was placed at the center of the port between the two conductors. The complex voltage phasor was then determined by integrating the electric field along this path.

$$\mathbb{V} = \int_{l} \vec{E} \cdot \overrightarrow{dl} \qquad (2)$$

In HFSS, V represents the complex voltage drop defined along the path l where the electric field is integrated. This value is computed for each frequency in the sweep. Since phase is not a critical factor in this analysis, the plots presented here display the magnitude (V_peak) of the complex voltage.

$$V_{peak} = |\mathbb{V}|. \qquad (3)$$

To enhance the accuracy of this calculation, an additional meshing operation was applied to the surface of the lumped port. This operation was configured to ensure a minimum of twenty meshing elements along the integration path. Moreover, the voltage quantity (V_peak) was incorporated as an additional convergence criterion in the HFSS adaptive meshing procedure, further ensuring the precision of the results.

3.2.Experimental Procedure

Experiments were conducted to validate the results of the HFSS simulations against physical test articles. Each Device Under Test (DUT) was placed in an anechoic chamber (Model 5247, ETS-Lindgren, Cedar Park, TX, USA) and exposed to radiation from an ultra-broadband 750 MHz–18 GHz horn antenna (Model 3115, ETS-Lindgren, Cedar Park, TX, USA). The horn antenna received a single-tone sinusoidal signal generated by a 25 GHz arbitrary waveform generator (AWG) (Model M8195A, Keysight, Santa Rosa, CA, USA), which was amplified by an 8 W wideband 1–22 GHz power amplifier (Model RFLUPA01G22GA, RF-Lambda, Carrollton, TX, USA). Measurements were taken using an 8 GHz mixed signal oscilloscope (Model WavePro 804-HD, Teledyne LeCroy, Chestnut Ridge, NY, USA). Although the simulations covered a frequency range of 0.1 to 10 GHz, the experimental setup was constrained to a range of 1 to 8 GHz. Figure 2 illustrates the complete experimental setup, including all equipment and fixtures.

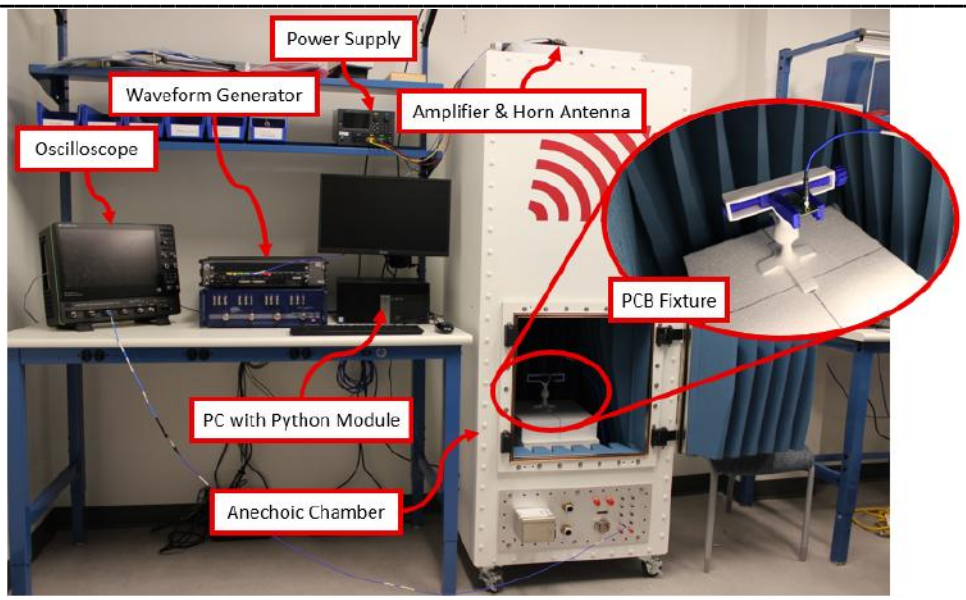

Figure 2. Experimental setup loop for making controlled induced voltage measurements. Signal generation is performed using a waveform generator, power supply, amplifier, and horn antenna. An anechoic chamber is used to mimic free-space conditions in a controlled environment, and a fixture is used for holding the device under test (DUT) at a consistent location and in a consistent orientation. Voltage measurements are performed using an oscilloscope, and a PC with a custom Python module is used to automate the testing procedure.

To compare experimental voltages with simulated voltages, it was essential first to ascertain the electric field strength at the Device Under Test (DUT). This electric field strength was then used to normalize and scale the experimental measurements for direct comparison to the simulation results. To determine the electric field strength, a thorough characterization of the chamber and testing setup was conducted.

In the following derivation, some quantities are relative and are denoted with associated units in square brackets. Quantities without units are absolute. Throughout the derivation, emphasis is placed on relative quantities because they simplify the calculation significantly. It should be noted that absolute voltage and power quantities can be converted to relative quantities using the logarithmic function, as demonstrated in the following equations:

$$P[\text{dBW}] = 10 \log (P) \tag{4}$$

$$V[\text{dBV}] = 20 \log (V) \tag{5}$$

To characterize the chamber, a second horn antenna was initially positioned on the test article platform inside the anechoic chamber. A Vector Network Analyzer (VNA) (Model C2420, Copper Mountain, Indianapolis, IN, USA) was then employed to measure the scattering parameters of the two-port network formed by the horn antennas. Specifically, port 1 was connected to the amplifier, and port 2 was connected to the second horn antenna. The scattering parameter S21 in this context quantifies the change in power received after passing through the cabling, amplifier, transmitting antenna, free space within the chamber, and

receiving antenna. It effectively describes the relationship between the transmitted power (PT) and the received power (PR):

$$P_{\mathrm{R}}[\mathrm{dBW}] = P_{\mathrm{T}}[\mathrm{dBW}] + S_{21}[\mathrm{dB}]. \quad (6)$$

We can now relate the received power to the peak output voltage using basic circuit theory:

$$P_R = \frac{V_{rms}^2}{R} = \frac{\left(\frac{V_{peak}}{\sqrt{2}}\right)}{50} = \frac{V_{rms}^2}{100} \quad (7)$$

where V_{rms} and V_{peak} are the RMS and peak output voltages, respectively. This equation is then adjusted to utilize relative quantities as described by Equations (4) and (5):

$$10 \log (P_{\mathrm{R}}) = 10 \log \left(\frac{V_{peak}^2}{100}\right) \quad (8)$$

$$P_{\mathrm{R}}[\mathrm{dBW}] = 20 \log \quad V_{\mathrm{peak}} \quad - 10 \log (100) \quad (9)$$

$$P_{\mathrm{R}}[\mathrm{dBW}] = V_{\mathrm{peak}}[\mathrm{dBV}] - 20[\mathrm{dB}]. \quad (10)$$

By combining Equation (6) with Equation (10) and solving for V_{peak} we establish a relationship among the output voltage, the transmitted power, and the forward voltage gain scattering parameter:

$$V_{\mathrm{peak}}[\mathrm{dBV}] = P_{\mathrm{T}}[\mathrm{dBW}] + S_{21}[\mathrm{dB}] + 20[\mathrm{dB}]. \quad (11)$$

Finally, the last step involves relating the output voltage to the incident electric field, which is achieved through basic antenna theory. Specifically, the Antenna Factor (AF) is a parameter that directly connects the voltage (V_{peak}) at the antenna port to the electric field strength (E) at the phase center of the antenna:

$$E[\mathrm{dBm^{-1}}] = V_{\mathrm{peak}}[\mathrm{dBV}] + |\mathrm{AF}[\mathrm{dBm^{-1}}]. \quad (12)$$

Note that the Antenna Factor is a parameter measured by the manufacturer during the characterization of a specific horn antenna. This data was obtained upon request.
By substituting Equation (11) into Equation (12) and solving for P_T we can calculate the power needed to generate a desired field strength at the Device Under Test (DUT):

$$P_r[\mathrm{dBW}] = E\ [\mathrm{dBVm^{-1}}] - S_{21}\ [\mathrm{dB}] - 20[\mathrm{dB}] - \mathrm{AF}[\mathrm{dBm^{-1}}]. \quad (13)$$

This value is subsequently employed to adjust the waveform amplitude. The current configuration can produce field strengths exceeding 30 V/m at the Device Under Test (DUT).

A Python module was created to automate the experimental testing process. This module prompts the user to input the desired frequency range and the desired field strength at the DUT. It then manages the Arbitrary Waveform Generator (AWG) for signal generation and the oscilloscope for signal measurement.

For each test frequency, the Python module executes the following procedures:

1. Utilizes Equation (13) to calculate the required transmitted power necessary to achieve the desired field strength at the specified frequency.
2. Interacts with the AWG component Object Model (COM) driver to generate a single-tone sinusoidal waveform with a peak-to-peak voltage determined in the previous step.
3. Interfaces with the oscilloscope, instructing it to wait until the signal stabilizes and then measure the peak-to-peak voltage of the output signal.
4. De-embeds the frequency response of the output cabling and the oscilloscope to account for their effects.
5. Normalizes the compensated output response to match the user-defined field strength.
6. Records the frequency and normalized voltage measurement.

After completing the test process for the entire frequency range, the module exports a CSV file containing each normalized induced voltage measurement along with its corresponding frequency across the entire test frequency range.

4. RESULTS

4.1. Radiated Susceptibility of Ideal Multilayer PCB

We start with an ideal multilayer PCB devoid of pads, traces, or vias, depicted in Figure 3. Figure 4 illustrates the stackup of the PCB, detailing the thickness of each layer. FR4, with a nominal permittivity of 4.27, serves as the dielectric substrate. It's important to note that this PCB shares the same stackup as the practical PCBs examined in the subsequent section. The PCB dimensions are 1" x 2", and all ground layers—top and bottom copper layers and inner ground plane—are interconnected using via stitching throughout the PCB. The power plane in each design is set back from the edge to accommodate via fencing. An ideal port with a 50 Ω impedance is positioned between the power and ground planes.

The incident plane wave's angle of incidence and polarization were determined by initially conducting an emissions simulation for the ideal stackup. Following the principle of reciprocity, peak coupling is expected to occur when the plane wave aligns based on peak emissions. Therefore, the internal port was excited, and the far-field radiation pattern was observed. This simulation revealed that the majority of energy is radiated in the positive and negative z directions, with the electric field (→E-field) polarized along the y-axis. Consequently, the plane wave was oriented accordingly, as depicted in Figure 3.

With all other parameters held constant, varying densities of via fencing were applied, and the voltage at the ideal port was measured. Figure 5 illustrates the different via fencing configurations, while Figure 6 presents the results obtained from these simulations.

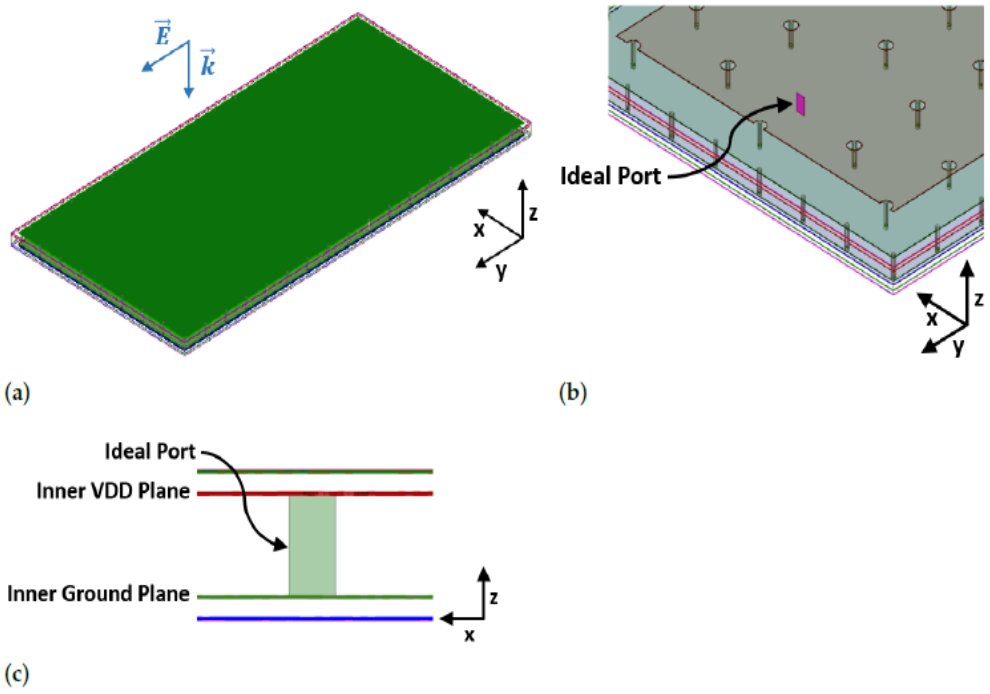

Figure 3. Four-layer ideal PCB: (**a**) 3D model with incident wave normal to the top of the board (−*z* direction) and $\vec{E}$-field polarized in the *y* direction, (**b**) 3D model port location, and (**c**) 2D model port location between inner planes.

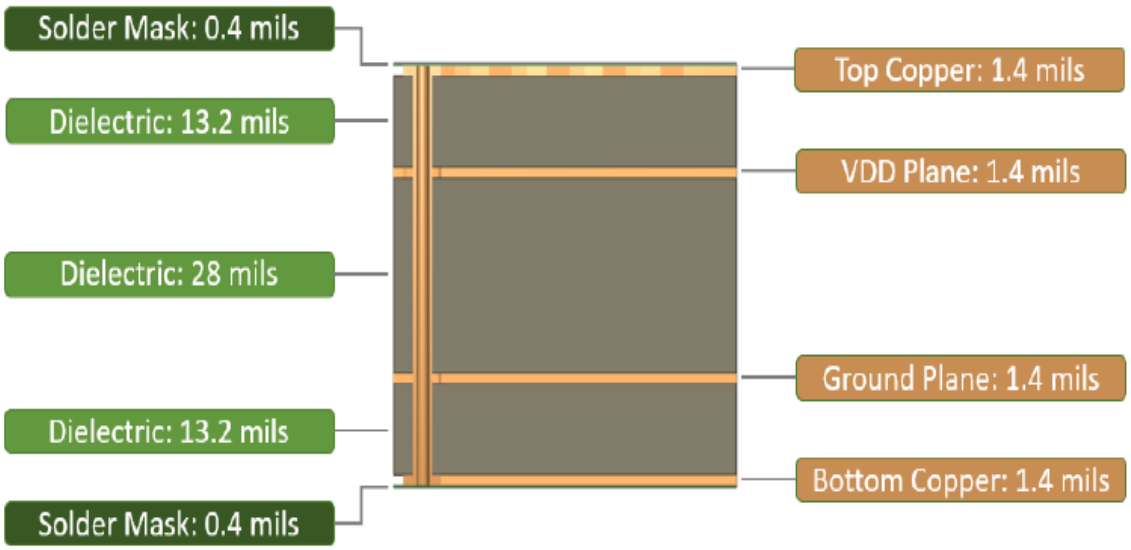

Figure 4. Four-layer PCB stackup including dielectric substrate, copper layers, and solder mask.

As depicted in the plot, there is a noticeable trend of decreasing voltage with increasing via density, which aligns with reduced emissions attributed to via fencing as documented in existing literature. Specifically, spacing the vias 20 mils apart results in a substantial reduction

of 35 to 45 dB in induced voltage across most of the frequency range compared to the design without via fencing. This improvement is significant; however, caution must be exercised in extrapolating these findings to dissimilar scenarios.

Additional angles of incidence and polarizations in the ideal case exhibit similar trends, but are omitted here for brevity. Unfortunately, due to the idealized nature of this design, these results cannot be experimentally validated. Nonetheless, given their consistency with other simulations and experimental tests on emissions, these data can be considered representative for an ideal PCB.

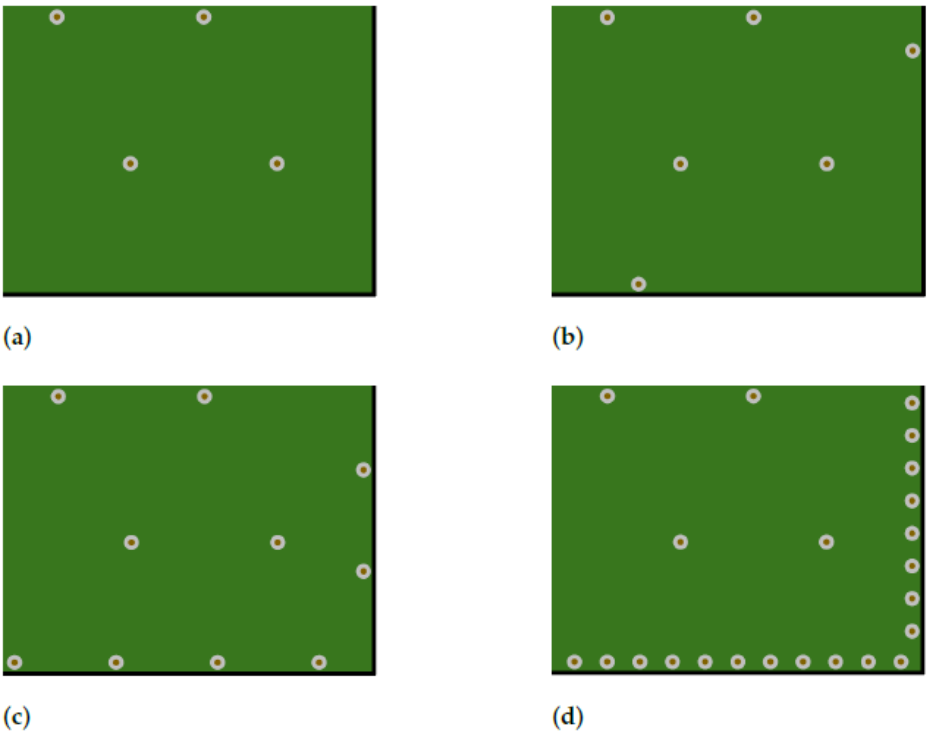

Figure 5. Variations in via fencing density around the perimeter of the PCB: (**a**) no via fence, (**b**) 400 mil via spacing, (**c**) 100 mil via spacing, and (**d**) 20 mil via spacing. Images show the corner of each PCB design for easy comparison. Note that in all cases, via stitching is present internal to the board to tie all ground layers together.

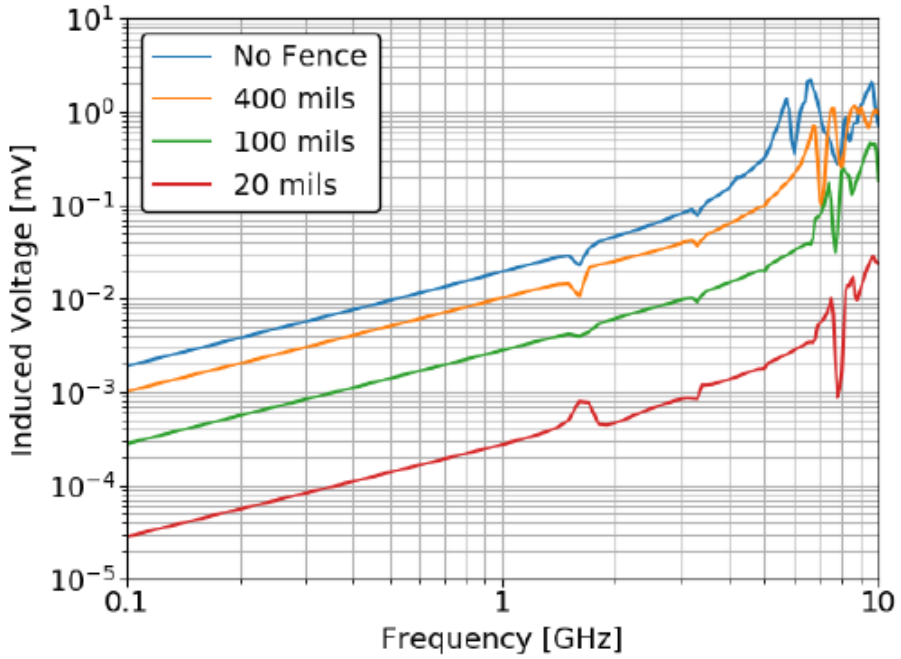

Figure 6. Induced voltage on the power plane of a four-layer ideal PCB with varying via fencing density.

4.2.Radiated Susceptibility of Practical Multilayer PCB

In the practical PCB design, component footprints and traces were introduced on the top layer. As depicted in Figure 7, separate simulations were conducted for three distinct angles of incidence:

- Case 1: Wave propagates in the negative z direction (-z) with the electric field (E-field) polarized along the y axis.
- Case 2: Wave propagates in the negative y direction (-y) with the E-field polarized along the z axis.
- Case 3: Wave propagates in the positive z direction (+z) with the E-field polarized along the y axis.

Each case was chosen based on emissions simulations and analysis of the far-field radiation pattern. By observing how the PCB emits radiation, we can identify which angles and polarizations result in maximum coupling. In this PCB setup, Case 3 represents the orientation with maximum emissions, followed by Case 1 and Case 2.

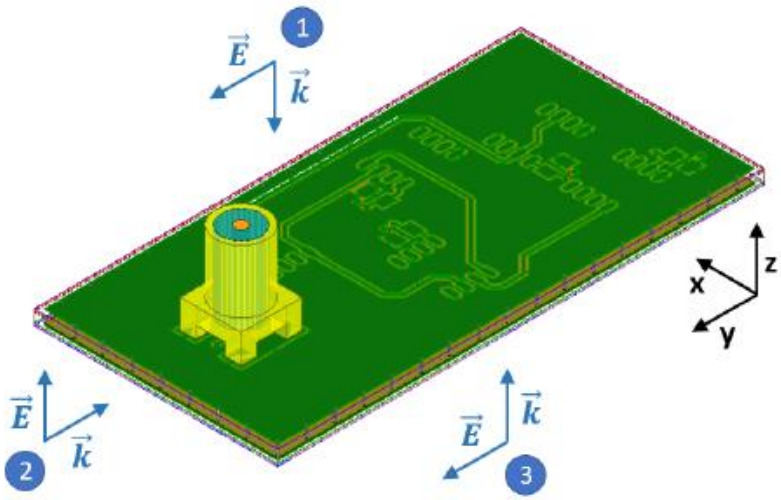

Figure 7. Four-layer practical PCB with two separate incident wave scenarios. The practical design includes component footprints and traces on the top layer as well as a surface mount sub-miniature version A (SMA) connector model for experimental measurements.

In practical PCB designs, component footprints and traces introduce openings in the top ground plane through which electromagnetic energy can enter. Additionally, an SMA connector is incorporated with its center pin directly connected to the power plane via a short trace and via. It's important to note that a surface mount SMA is used here instead of a through-hole connector to better simulate a real component with a power pin. The SMA connector is included in the simulation to closely mimic experimental testing conditions wherever feasible. Once again, the density of via fencing is varied, and the voltage at the SMA port is measured. The following sections present both simulated data and experimental data, accompanied by relevant discussions.

4.2.1. Practical PCB Simulation Results

The practical PCB designs were simulated using the same procedure and settings as the ideal designs. Figure 8 displays the simulated results for each angle of incidence and via fencing density. Upon reviewing the plots in Figure 8, several observations can be made, highlighting notable differences from the ideal case.

Firstly, it is evident that in the practical design, resonant modes are more pronounced, especially at lower frequencies. The induced voltage is also significantly higher across most of the frequency range, indicating that more electromagnetic energy reaches the power plane. For instance, in Figure 8a, the peak voltage (approximately 3 mV) suggests that if scaled by a typical high intensity field strength (10 kV/m), the circuit would experience an induced voltage of 30 V.

Furthermore, a notable observation is that there is minimal variation among the different densities of via fencing. At frequencies where deviations occur, via fencing generally reduces coupling, but occasionally it results in increased coupling. In regions where via fencing is effective, it can achieve a reduction in induced voltage ranging from 5 dB to 20 dB (as indicated by shaded areas in Figure 8). While this improvement is not as extensive as in the ideal case and doesn't cover the entire frequency range uniformly, it still

represents a significant enhancement that could mean the difference between permanent damage and temporary malfunction.

Another important finding is the limited discernible difference among each angle of incidence and polarization. As anticipated, the amplitude varies to some extent because certain angles and polarizations can more effectively excite resonant modes. However, the differences in the effectiveness of via fencing densities remain relatively consistent across all cases. This consistency was also observed in additional angles of incidence and polarizations beyond the three cases presented here.

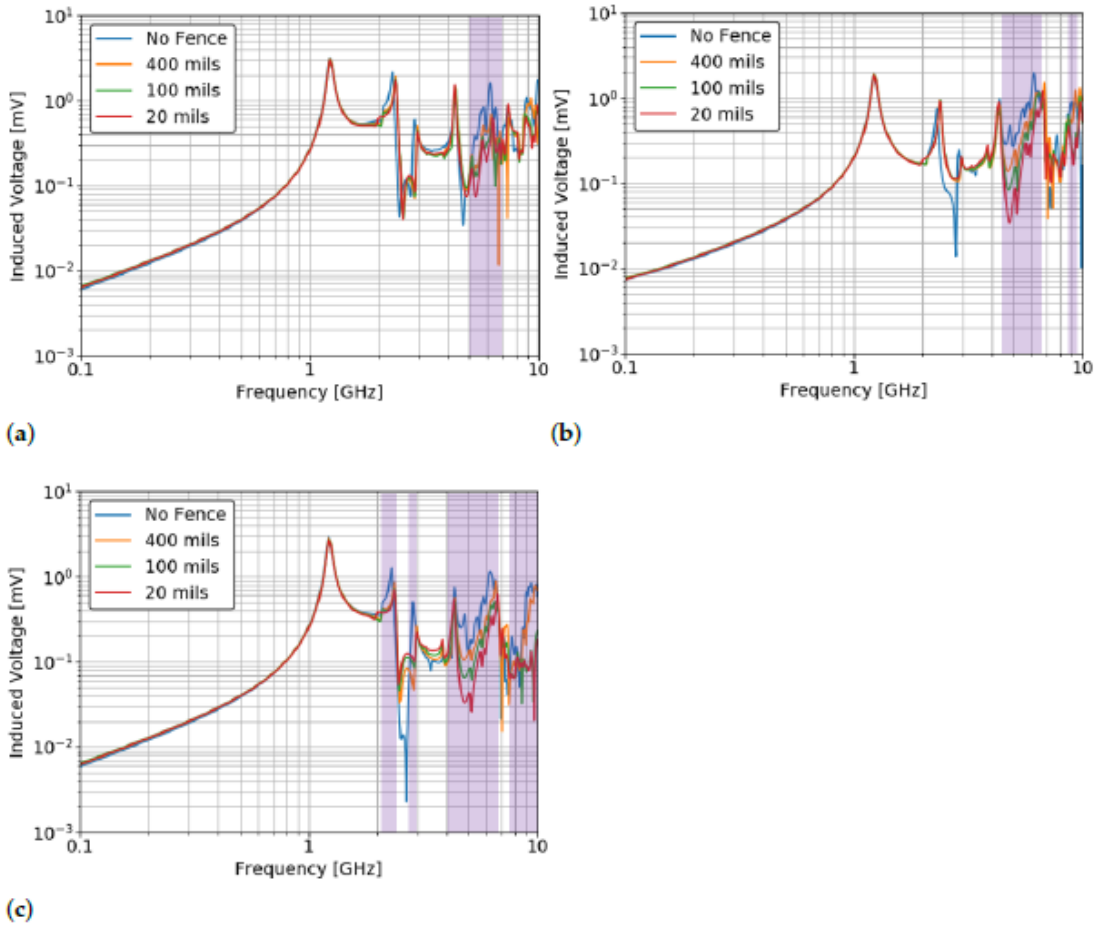

Figure 8. Induced voltage on the power plane of a four-layer practical PCB with varying via fencing density: (**a**) plane wave propagating in the negative *z* direction (Case 1), (**b**) plane wave propagating in the negative *y* direction (Case 2), and (**c**) plane wave propagating in the positive *z* direction (Case 3). The shaded regions indicate where via fencing reduces induced voltage.

Based on these observations, it is evident that in the practical case examined here, the primary coupling mechanism involves electromagnetic energy reaching the power plane through openings in the top layer. Interestingly, similar outcomes were achieved when the entire PCB edges were covered with perfect electric conductor (PEC) sheets, indicating minimal energy transfer through edge coupling. This finding contrasts with

expectations drawn from previous studies on emissions and via fencing, which suggest that via fencing could substantially reduce coupling, akin to the ideal scenario presented earlier. However, in practical scenarios, this reduction may not always occur.

Further validation of this conclusion was obtained through transient simulations of practical designs. Animated field simulations clearly illustrate that energy enters the power plane through narrow openings in the top layer. While energy leakage does occur through the PCB edges, the dominant behavior involves energy ingress via the top layer. This observation holds true even for incident fields at the edge (Figure 8b) and bottom (Figure 8c) of the PCB.

To illustrate this transient behavior, the trace layout of the practical PCB design was adjusted to create three distinct configurations, each with unique openings in the top layer. Subsequent transient simulations plotted surface current density on the power plane, confirming consistent behavior with previous findings. The simulations revealed high surface current density near traces and pads, precisely aligning with locations of the top layer openings (Figure 9).

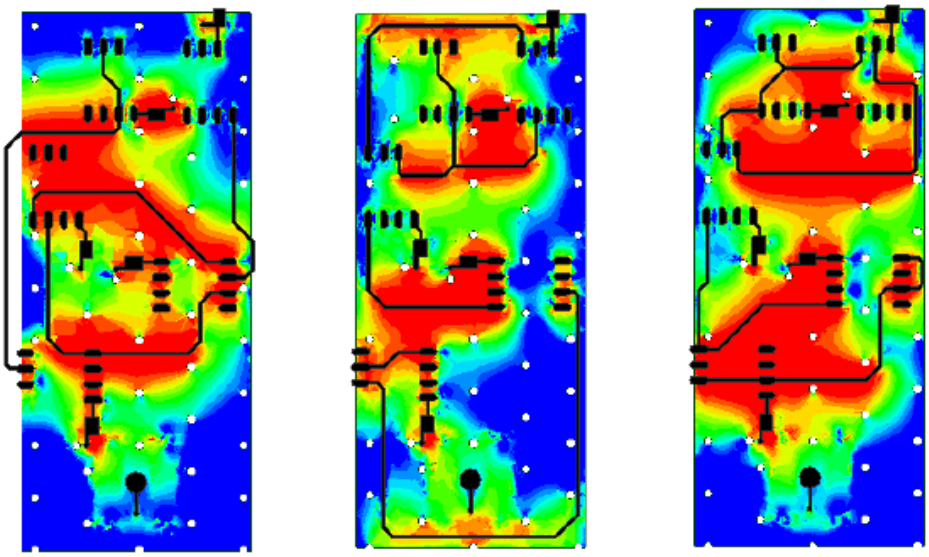

Figure 9. Power plane surface current density for varying trace routing layouts: (**a**) Layout 1, (**b**) Layout 2, and (**c**) Layout 3. Pads and traces are colored black to indicate where openings in the top layer exist. The plots show that surface currents are first excited where openings exist, indicating that electromagnetic energy reaches the power plane through these openings.

4.2.2. Practical PCB Experimental Results

While HFSS provides valuable field visualizations, model validation remains crucial whenever feasible. Experimental data not only validate the model but also account for factors that are challenging to accurately simulate or would require impractical simulation times. To validate the practical PCB design, four identical PCBs were manufactured with varying densities of via fencing on an FR4 substrate with a nominal permittivity of 4.27. Figure 10 displays images of these PCBs, showcasing the different via fencing densities.

For experimental verification, the procedure outlined in Section 3 was employed. Figure 11 presents a comparison between simulated and experimental data for a scenario where the

wave propagates in the negative z direction (Case 1). Additionally, Figure 12 separates the simulation and experimental curves, providing a detailed comparison of via fencing performance. Figure 11 contributes to model validation insights, whereas Figure 12 offers clarity on the effectiveness of via fencing.

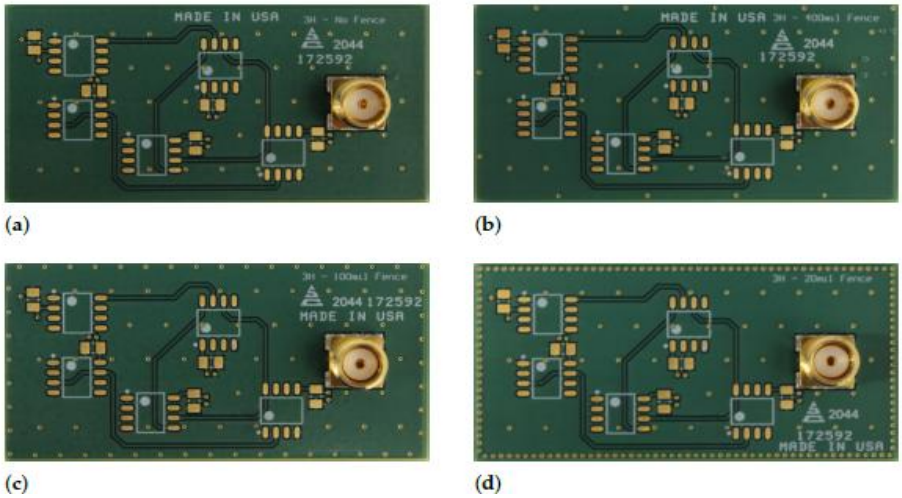

Figure 10. Variations in via fencing density around the perimeter of the fabricated PCBs: (**a**) no via fence, (**b**) 400 mil via spacing, (**c**) 100 mil via spacing, and (**d**) 20 mil via spacing. Note that in all cases, via stitching is present internal to the board to tie all ground layers together.

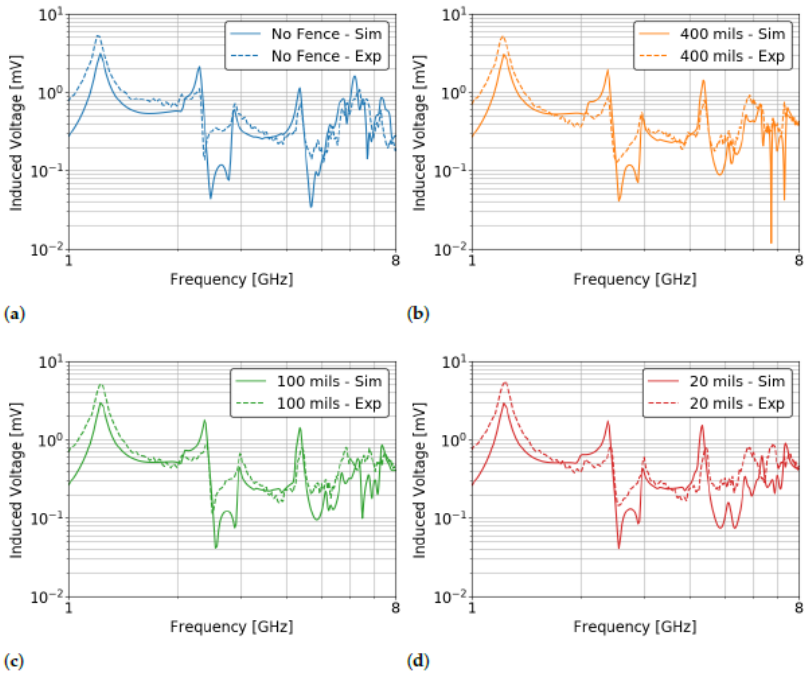

Figure 11. Comparison of simulated vs. experimentally measured induced voltage for each via fencing variation: (**a**) no via fence, (**b**) 400 mil via spacing, (**c**) 100 mil via spacing, and (**d**) 20 milvia spacing. The experimental data validate the modeling results and give further proof that the dominant coupling mechanism is not at the PCB edges.

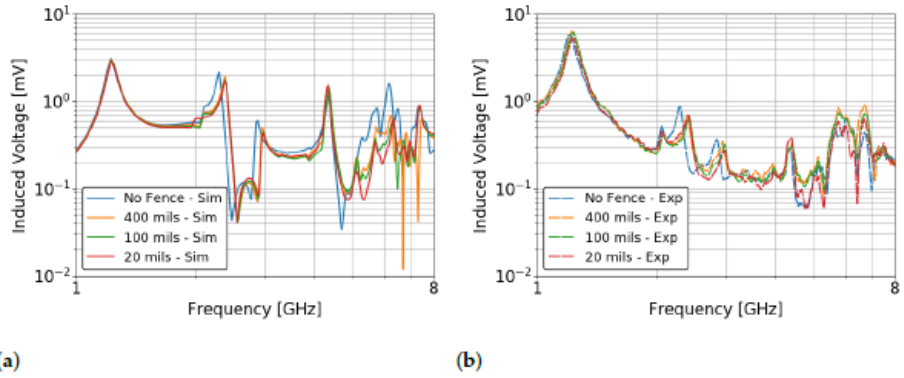

Figure 12. Comparison of simulated vs. experimentally measured induced voltage for a plane wave propagating in the negative *z* direction (Case 1): (**a**) simulation and (**b**) experimental. The experimental data deviate slightly from the simulation data but similarly demonstrate that via fencing density does not dramatically affect coupling.

As shown in Figure 11, the experimental measurements closely align with the simulated data. Across each variation in via fencing density, the induced voltage exhibits similar magnitudes and resonant peaks at comparable frequencies. Expectedly, there are slight deviations attributable to several factors. The model's nominal dimensions differ from actual fabrication measurements; the boards were found to be slightly thicker than nominal, and inner layer spacing varied. Moreover, the model assumes a constant permittivity for FR4, whereas in reality, permittivity varies with frequency. The presence of the experimental measurement cable, not accounted for in the model, also influences the PCB's near-field characteristics. Despite these differences, the overall agreement between simulation and experiment is robust, validating both approaches in the context of radiated testing challenges.

In Figure 12b, the experimental data further reveals minimal variation in induced voltage among different via fencing densities. Similar to simulation results, via fencing occasionally reduces coupling while in other instances it increases it. However, across different angles of incidence, variations with via fencing show more noticeable reductions in induced voltage, albeit by a modest margin.

5. DISCUSSION

The research presented here offers unique insights into board-level coupling mechanisms and mitigation techniques, which are crucial for advancing understanding in this field. Contrary to previous assumptions regarding the efficacy of via fencing, the data indicate that via fencing does not significantly mitigate coupling in practical PCBs. However, slight improvements were observed at specific frequencies, making via fencing a cost-effective addition to PCB designs. In contrast, edge plating, though more costly, did not provide additional benefits beyond traditional via fencing.

It is essential to emphasize the limited applicability of these findings to other scenarios. The observed behavior is likely specific to stackups where a power plane is adjacent to an outer signal layer, allowing direct excitation of surface currents on the power plane by electromagnetic energy. Different stackups may exhibit different coupling behaviors.

For instance, a six-layer PCB with a shielding layer between the top signal layer and the inner power plane might shift the dominant coupling mechanism to edge coupling. This scenario could potentially benefit from high-density via fencing for effective mitigation.

Future research will explore such scenarios and expand investigations to include parameters like power plane pullback, layer separation, board thickness, substrate permittivity, and losses. These efforts aim to develop comprehensive PCB design guidelines tailored for systems operating in High-Intensity Radiated Fields (HIRF) environments.

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