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Research Papers



A NEW SOFT-SWITCHING ACTIVE CLAMP SCHEME FOR FULL-BRIDGE ISOLATED CURRENT FED DC-DC CONVERTER FED DRIVES

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Abstract

This paper presents on a new high power full bridge isolated current fed dc/dc Converter with an active clamp. A proposed current fed dc/dc converter with high efficiency and voltage boosting capability is designed for use in the interface between a low voltage fuel cell source and a high voltage dc bus for inverters.ZVS scheme in all active switches is achieved for using a soft switching scheme. The switching losses and the conduction losses are reduced and the performance of the drive system should be increased from the proposed model. The proposed converter system is controlled by SPWM Technique. The simulation results are carried out and presented.

Keywords: Active clamp, Leakage inductance, Three–phase dc–dc converter, Three–phase pulse width modulation (PWM), Voltage transfer ratio, Zero–voltage switching (ZVS), MOSFET (metal oxide semiconductor field effect transistor).

1. INTRODUCTION

FUEL CELLS are identified as a future source of generating energy due to their efficient and clean energy characteristics; furthermore, they produce low-varying dc voltage in the range of 30–60 V for static power application such as residential use. For static fuel cells, the power conditioning system usually consists of a low-voltage fuel cell as the primary source, a dc/dc converter to obtain isolated high voltage, and a dc/ac inverter to connect commercial ac voltage. Since a dc/ac inverter supplies power into a 220–V ac utility, an isolated dc/dc converter has to convert low varying dc voltage to high constant dc voltage at around 370 V. Therefore, a dc/dc converter with a high voltage ratio is needed, and a transformer is usually employed for boosting voltage as well as isolation. However, high leakage inductance in the transformer leads to trouble such as voltage spikes and electromagnetic noise. In order to achieve a high voltage to pology for all single–phase application. In addition, a soft-switching active clamp scheme has been proposed to minimize turn-off losses in the clamp switch. These converters have been shown to perform quite well, but the single–phase circuits face severe components stress and degraded efficiency for higher power levels.

2. PROPOSED CURRENT FED DC/DC CONVERTER SYSTEM CONFIGURATION:

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Fig.1. Proposed current fed dc/dc converter system configuration

current-fed converter is divided into a three-phase full-bridge converter configured as six main MOSFETswitches (S1–S6) for three-phase dc/ac conversion, one auxiliary MOSFET switch (SC) and clamp capacitor CC for the active clamp, and a dc boost inductor Ldc acting as a current source. The main switches and auxiliary clamp switch performZVS through the use of resonance between leakage inductances of the three-phase transformer, clamp capacitor, output capacitances at MOSFET switches, and stray capacitances in the transformer. Therefore, it reduces switching losses and leads to a highly efficient, isolated voltage boost converter. It should be noticed that the three-phase transformer can be given the form of three discrete single-phase transformers connected in deltadeltawinding or a three-legged transformer commonly used in the utility line. Advantages of employing a current-fed converter with an active clamp in the dc/ac stage are as follows: the voltage across the switches is well clamped (i.e., no voltage overshoot), all switches operate with ZVS, no ancillary snubber is required in either the primary or secondary sides, requirements for the output rectifier's speed are less stringent due to zero current switching, and input current generated from the fuel cells or a photovoltaic source is continuous, with small ripples.



3. PROPOSED PWM STRATEGY WAVEFORM

Fig.2.(a) Circuit simplified through replacement of the three-phase transformer with leakage inductance Llk

The delta-delta wound three-phase transformer is represented by its three leakage inductances Llk and its output voltage Vo on the secondary side is referred to on the primary side as Vo'. It is assumed clamp capacitor CC and output capacitor CO are infinite in value; these are referred to by voltage sources VC and VO, respectively. The boost inductor Ldc can be replaced by a current source Id during each switching period. Fig. 2(b) shows the ideal current waveforms of phase A current IA and clamp currentISc, the gating signals for main switches S1–S6, and clamp switch SC together with corresponding working switch pairs. Duty ratio D is defined as an interval when all main switches are turned on and boost inductor Ldc charges energy from input source Vd. Major features of the proposed converter include: 1) increased power transfer for switches with the same current and voltage rate, when compared to single-phase solutions. 2) an achievement of ZVS in active switches through a single common active clamp branch and zero current switching in rectifier diodes; 3) lowering of the transformer turns ratio by using boost characteristics inherited by current-fed boost type; 4) a reduction in the size of the input dc inductor and elimination of the output filter inductor by increased effective switching frequency; and 5) a reduction in conduction loss through distribution of rms current among

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per-phase switches and transformer windings, when compared to a single-phase converter for the same power ratings.



Fig.2.(b) Ideal waveforms of the proposed converters

4. THREE-PHASE CURRENT FED DC-DC CONVERTER ANALYSIS:

The steady-state clamp capacitor voltage is determined using the inductor Ldc voltage-second balance; the formulas (1) and(2) for the ideal clamp capacitor voltage VC and the ideal output voltage VO are repeated here for comparison with real values

$$V_C = \frac{V_d}{1 - D}$$
$$V'_O = \frac{V_O}{n}$$
$$V_C = \frac{V_d}{1 - D}$$
$$V_O = \frac{nV_d}{1 - D}.$$

Due to current-second balance in the clamp current ISC in the steady state, average values of ISc during t0-t2 equals zero given as

$$I_{Sc(AVG)} = \frac{1}{T_S} \int_{t_0}^{t_2} \left(I_{d(t-t_0)} - \frac{I_{d(t-t_0)} - I_{d(t-t_2)}}{(1-D)T_S} - I_m - \frac{V_C - V'_O}{2/3L_{lk}} \right) dt = 0$$

where Id(t=t0) is the dc inductor current Id at t = t0, Id(t=t2) is the dc inductor current Id at t = t2, Im is magnetizing current given as

$$I_m = \frac{-V_O'(1-D)T_S}{2L_m}$$

By substituting (10) and (12) into (11), expression for output voltage VO is derived as

$$V_{O} = \frac{n}{(1-D)(1+L_{lk}/L_{m})} \left(V_{d} - \frac{2P_{O}2/3L_{lk}}{\eta V_{d}T_{S}} \right)$$
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The output voltage decreases from the ideal value in (10); this is mainly caused by leakage inductance Llk, output powerPO, and overall efficiency η . The efficiency η takes all losses into account, such as the conduction and switching losses of the switches, dielectric losses of capacitors, copper and ironlosses of the transformers, etc. Therefore, leakage inductance Llk reduces the overall voltage transfer ratio. The normalized output voltage is defined as

$$\tilde{V} = \frac{V_O}{nV_d}$$
, $V_C = \frac{V_O}{n} + \frac{2(P_O/\eta V_d - I_m) 2/3L_{lk}}{(1-D)T_S}$

Clamp capacitor voltage increases from the ideal value in(9) through the effect of inductance Llk output power PO, and overall efficiency η ; this means the maximum voltage stress Authorized licensed on the clamp capacitor and the main switches increases as Llk increases. The normalized clamp capacitor output voltage is defined as

$$\tilde{V}_C = \frac{nV_C}{V_O}$$

The minimum Llk value necessary for ZVS to turn on is

$$L_{lk} \ge \frac{\left(2V_d V_O / (1-D)n - V_d^2 / (1-D)^2\right) C_S}{\left(P_O / \eta V_d + V_d DT_S / 2L_{\rm dc} + V_O (1-D)T_S / 2nL_m\right)^2}$$

where CS = CS1 + CS6 + CSc (at S1 - S6 on interval). The required Llk for ZVS operation is determined by making the energy stored in leakage inductance Llk be greater than compound stray CS during resonant interval out of t2–t3.

5. SIMULATION RESULTS AND DISCUSSION

The proposed model is simulated by using mat lab/simulink. The output results are shown below.



rig 3.1 rioposed unree phase DC – DC Converter base drive system

The dc voltage generated in the photovoltaic array is simulated for 440 volt is applied to the inverter and the result is analyzed with the resistive load(normally the grid system consist of unity power factor so the resistive load is used for simulation analysis)

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Fig 5.2 DC intput voltage This simulation model consist of the two MOSFET switches with an freewheeling diodes is linked with an PWM inverter, the output is linked to an load along with the HERIC circuit and the filter across the terminal. The waveform is obtained from different part of the model and shown below, T h e output voltage is obtained across the load consist of low distortion.

INPUT VOLTAGE AND CURRENT WAVEFORM





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Fig 5.3 output voltage across load terminals

6. CONCLUSION:

A new three-phase dc/dc converter and PWM strategy have been proposed in this paper. The proposed converter would haveZVS in all active switches. This would be achieved through using the common active clamp branch and zero current switching in the rectifier diodes, and thus producing discontinuous current Conduction. Further, the converter has been shown to be capable of increased power transfer due to its three-phase power configuration, and it reduces the rms current per phase, thus reducing the conduction loss as well. Moreover, a delta-delta connection on the three-phase transformer provides parallel current paths and reduces conduction loss in the transformer windings. Reductions in both the switching and conduction losses results in converter efficiency of above 93%. Inherent voltage boost characteristics of the current-fed converter increase the voltage transfer ratio in addition to the transformer turns ratio. Further, it has been shown that the proposed converter can be realized with smaller sized filter components, which leads to higher power density. These advantages make this converter suitable for low dc voltage renewable energy sources such as fuel cells and photovoltaic array.

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