Vol 3 Issue 2 March 2013

Impact Factor : 0.2105

ISSN No : 2230-7850

Monthly Multidisciplinary Research Journal

Indian Streams Research Journal

Executive Editor

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IMPACT FACTOR : 0.2105

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RNI MAHMUL/2011/38595 **ISSN No.2230-7850**

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Indian Streams Research Journal
Volume 3, Issue. 2, March. 2013
ISSN:-2230-7850
Available online at www.isrj.net
ORIGINAL ARTICLE

ANALYSIS AND DESIGN OF DIGITAL RECEIVER USING MULTI-BIT FFT ALGORITHM IN RADAR EW APPLICATIONS

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Abstract:

In radar EW applications, the problem of simultaneous signal remains as a problem of DIFM receiver ,which is being solved using the digital receiver.. A low SNR signals can be processed only using the digital receiver which is not possible using the analog receiver. These digital receivers are well suited to perform as wide band Channelizer, tunedsuperheterodyne receiver, compressive receiver functions .In this paper we have analysed and studied the advantages of designing the digital receiver using monobit and multibit fft algorithms ,simulation results of algorithms are presented.

KEYWORDS:

digital receiver,EW(electronic warfare),SNR,FPGA,kernals.

INTRODUCTION:

Various Electronics Warfare (EW) receiver technologies are in use for detection and parameter measurements of radar signals. These EW receivers are

i. Crystal Video Rx
ii Superhetrodyne Rx
iii. Instantaneous Frequency Rx (IFM)
iv. Channelized Rx
v. Micro scan Rx
vi. Bragg Cell Rx
vii. Homodyne Rx &
viii Digital Rx.

The EW receiver technologies for Crystal video, Superhetrodyne, Channelized and IFM Rx are well matured and employed in EW systems designs. Micro scan & Bragg cell receiver arenotwell matured. Digital receiver are being employed in present EW systems. Earlier Digital Receiver could not be employed in EW system design, due to non availability of Analog-to-Digital converter(ADC) at radar frequency. Also, real time digital signal processors are not available. Presently, technological advances in RF to Digital converter are available in several GHz frequencies. Moreover digital design implementations are becoming more attractive with the availability of high density Field Programmable Gate Array's (FPGA's). High speed ADC, high gate density FPGA's and dedicated high speed signal processor availability, make the radar EW system design to employdigital receiver in radar EW system.

For wide band RF application in the radar EW using digital receiver employ down converter

Title : ANALYSIS AND DESIGN OF DIGITAL RECEIVER USING MULTI-BIT FFT ALGORITHM IN RADAR EW APPLICATIONS
Source:Indian Streams Research Journal [2230-7850] M.L.S.N. SWARAJYA LAKSHMI , D.S RAM KIRAN AND NIRANJAN PRASAD
yr:2013 vol:3 iss:2

followed by high speed , high bandwidth ADC and a signal processor. The signal processor for radar EW System application use real time digital spectrum analysis available in a special hardware configuration and in customized FFT algorithms(1). State of the art design of ADC dictate the performance capability and evolution of digital receiver. Presently, digitization of direct RF signal upto several giga hertz's are available.

2. DIGITAL RECEIVER FOR RADAR EW SYSTEMS:

There are certain design features of digital receivers that has become attractive for use in radar EW system over other receivers processing techniques. They are:

i. Digitized data can be stored for a long period of time and detailed analysis of the signal.
ii. Flexible signal processing algorithms are possible to obtained the desired information directly from digital data.
iii. Real time digital spectral analysis is possible using special hardware and customized FPGA Intellectual Property (IP) cores.

2.1 Advantages of Digital Receiver:

There are certain distinct advantages in using digital receivers for radar EW system. They are

1. Simultaneous signal processing capability
2. Reduced RF/ analog drift and bias.
3. Accurate radar parameters estimations.
4. Re-programmability of processor software for future requirements without changing the Hardware.
5. Significant system size, weight and volume reduction.

3. CONFIGURATION OF DIGITAL RECEIVER:

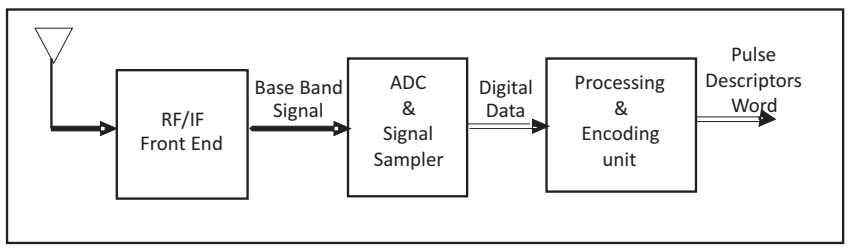

Fig.1: Basic block diagram of Digital Receiver

Digital receiver consists of three major functional units, namely

RF/IF front end unit
Signal sampling unit
Signal processing unit

3.1 RF/IF front end:

Usually the RF frequency of operation of the radar EW system is in the range of 0.5-40GHz.

Since ADC is not available in these wide frequency ranges, the input frequency is channelized and converted to a base band frequency in a RF/IF front end unit. The purpose of RF/IF Front end is to convert the RF signal to base band signal. The conversion is required, because, wide band RF signal directly cannot be converted to digital data, since ADC is not available for the above RF range.Conversion from RF to base band signal can be achieved either by channelizer followed by downconverter or directly using super heterodyne technique. One typical example used as RF front end of digitalreceiver is shown in Fig2.

The RF signal intercepted by the antenna is given to the RF front end section. RF section consists of RF amplifiers, mixers, filters and base band amplifiers. RF signal of0.5-40GHz is converted to base band

frequency, say 750-1250MHz by mixing the RF with the proper LO signal and then amplified by an intermediate frequency amplifier. Further a base band pass filter is used which will reject any inter modulation products and harmonics at the output of the baseband signal.

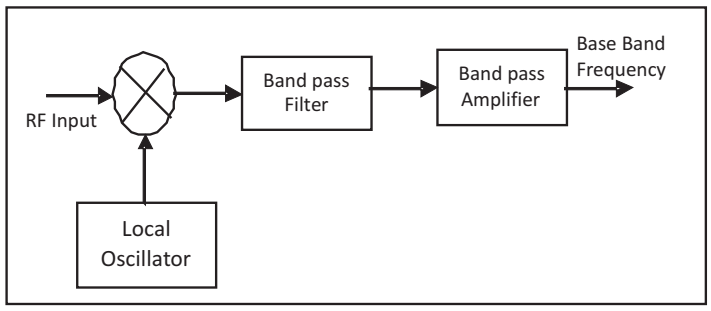

Fig.2:A Typical RF Front End Unit

3.2 ADC and Signal Sampler Unit:

The output from the RF front end i.e. base band signal is given to ADC and signal sampler unit. The analog to digital converter is selected to cover the input analog bandwidth of the base band signal. The function of ADC is to convert the analog signal to digital stream of discrete levels. The analog signal is sampled at regular interval to convert the signal into discrete time signal. Subsequently, its sampled amplitude will also be approximated to different amplitude level, which will be encoded in digital bits. Higher the number of bits, finer will be the amplitude quantisationlevel. Usually, sampling accuracy is determined by the highest frequency content of the base band signal. For re-construction of the information from ADC, sampling rate is chosen as per Nyquist criterion (2).

3.3 Dynamic Range of the ADC:

The dynamic range of ADC is approximated by
DR = 20 log2 2^N = 6N
Where N= number of bits.

With an 8 bit ADC , a dynamic range of 48dB can be achieved and this may further be increased by increasing the bit resolution of the ADC. Proper formatting of the data is also required before the data is given to the signal processing section. Generally for data match , ADC data is used and then given to FPGA or DSP for processing.

4. PROCESSING & ENCODING UNIT:

Processing and encoding unit, process the digitized signal for spectrum analysis and Parameter estimation. Digital signal processing (DSP) algorithm is implemented in this unit. The hardware for implementation of the DSP algorithms varies from the type of application intended.

There are three types of hardware employed for the implementation. They are

(1) Microprocessor
(2) DSP processor
(3) FPGA or Programmable devices

4.1 Microprocessor:

The ADC data can be given to the microprocessor i.e. Intel P-IV or IBM Power PC etc, for the processing. The microprocessor is a generic processor which are based on RISC or CISC architecture, has only one ALU unit. The instruction will be read by microprocessor, get decoded and subsequently executed. This type of architecture is more suitable for the embedded application. The DSPalgorithm

requires many multiplier and accumulator, which is not supported by the microprocessor architecture. Hence it will take more time for processing the DSP algorithms, which in many cases is not desirable. This is the main reason for microprocessor not being used in any of the DSPapplication.

4.2 DSP Processor:

DSP techniques are used by DSP processor from M/s Texas Instrument (TI320C6701,6201etc.) or M/s Analog Devises(TS101,TS201 etc) is mostly selected for EW applications. The main difference between microprocessor and DSP processor is of MAC(Multiply and accumulate). MA Cooperation in DSP processor is done in one cycle, which will make the processing faster than with microprocessor.

An architecture of TMS320C6701 floating point DSP processor is shown in Fig.3. The CPUcontains:

a. Program fetch unit
b. Instruction dispatch unit
c. Instruction decode unit
d. Two data paths, each with four functional units
e. 32 number 32-bit registers
f. Control registers
g. Control logic
h. Test, emulation, and interrupt logic

The program fetch, instruction dispatch, and instruction decode units can deliver up to eight 32-bit instructions to the functional units every CPU clock cycle. The processing of instructions occurs in each of the two data paths (A and B), each of which contains four functional units (.L, .S,.M, and .D) and 16 32-bit general-purpose registers.

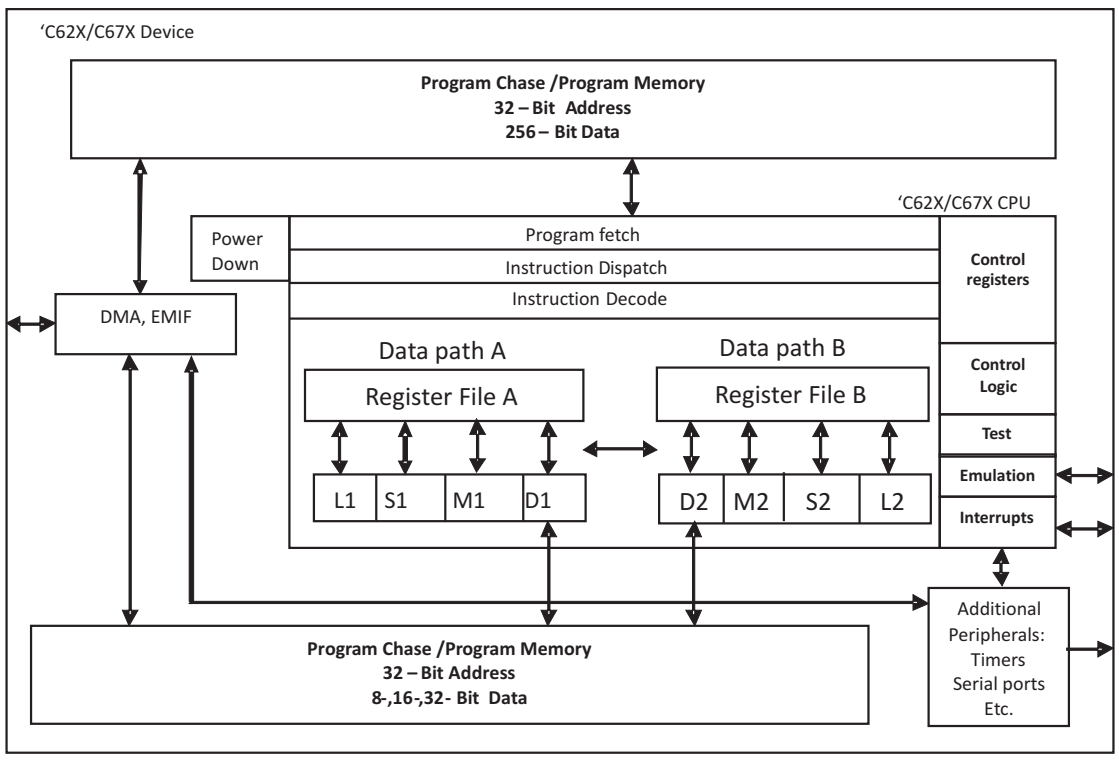

Fig.3 :TMS320C62x/C67x Block Diagram

4.3 Digital Signal processing Using the FPGA:

The Field Programmable Gate Array (FPGA) are getting more popular for DSPapplication where

the processing time required is of the order of a nanosecond. FPGA is more suitable for Radar EW application, where processing time is one of the important requirements. The present day FPGA has millions of gates and very high processing speed. Apart from that, special FPGA's are available which suits the DSP application like Xilinx Virtex SX series FPGA. These FPGA's has many number of multiplier, distributed memory for storing the computation, which suite for the DSP application. Hence, the Digital Receiver which is being configured for Radar EW application is based on the FPGAprocessing.

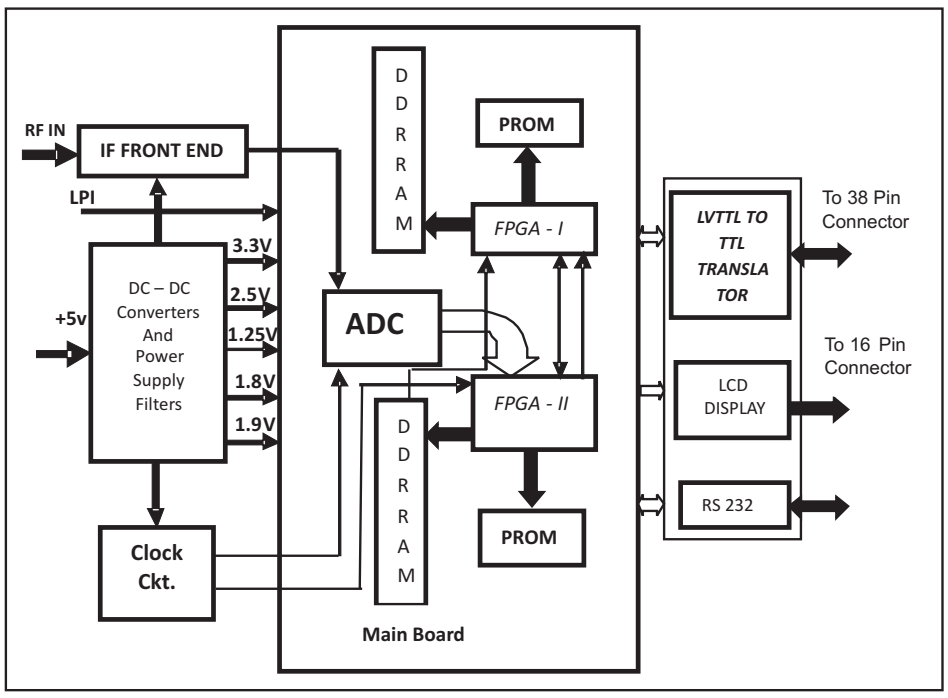

Fig.4: Typical configuration digital receiver using FPGA

5. CONFIGURATION OF DIGITAL RECEIVER SUITABLE FOR RADAR EW APPLICATION:

The main difference in conventional digital receiver and that applicable to EW is that in EW, the parameters measured are to be carried out on a single received RF pulses. There are many possible configurations for digital receiver as per the specific requirements(3). Two such algorithms are explained.

1. Monobit Digital Receiver
2. Multibit Digital Receiver

5.1 Monobit FFT Algorithm:

This is the key component of the design. The purpose is to eliminate multiplication and keep only adders and subtractors in the discrete Fourier transform chip design. The DFT can be written as $X(k) = \Sigma X(n) \exp(-j*2*\pi*k*n / N)$. $n = 0$ to $N-1$, $k = 0$ to $N-1$. eq(1)

Where $j = \sqrt{(-1)}$ and N is the total number of sampled input points. In this equation the result is obtained as a result of multiplication of two functions: the input x (n) and the kernel $\exp(j*2*\pi*k*n/ N)$. If either one of these two functions is one bit i.e. + 1 or − 1, the operation requires only addition, shown in figure 1. This is the principle of Monobit Algorithm. In Multibit design the kernel function is approximated to nearest whole numbers i.e., all the multiplication operations are eliminated by simple left shift operations, this is mapped to a time-decimated radix-2 FFT algorithm. The FFTcontains 256 inputs. Here 32 kernel points are used instead of 4 kernel points, due to which the rounding error is reduced and the result obtained is of high instantaneous dynamic range.

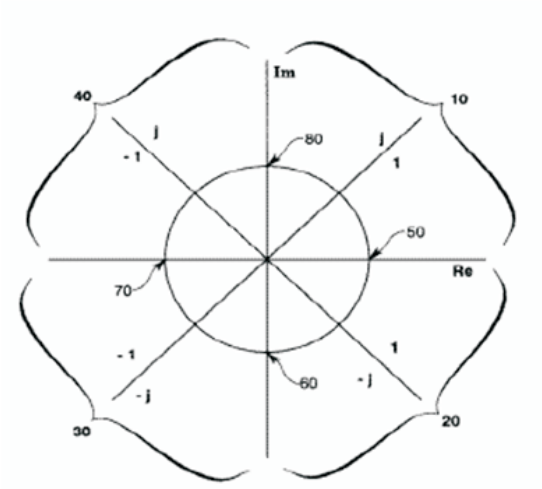

Fig.5: Monobit kernel approximation

5.2 Multibit FFT Algorithm:

The unit circle is scaled by powers of two i.e., it can be scaled by 2, 4 and so on. We only select powers of 2 as in hardware, multiplication by these numbers simply means shifting the multiplicand to the left and padding zero's on its right side i.e., scaling by 2 is shifting left one bit and appending one zero right side and for 4 shifting left twice and appending two zeros on the right side. Scaling the twiddle factor by 2 and rounding to the nearest whole number, angle reduces from 45º to around 20° due to which the rounding errors are reduced and dynamic range increases to some extent. Here the number of kernel points increases from 4 to 16. The design is performed by scaling the unit circle by 4 to have the better results.

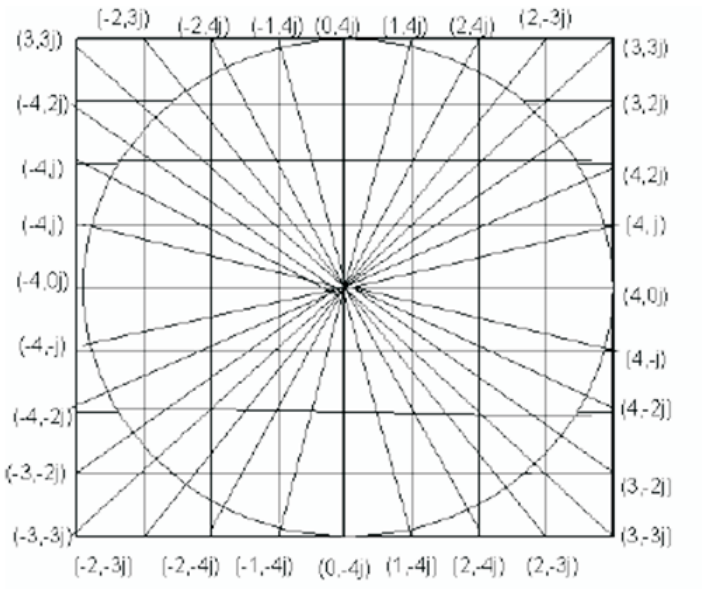

Fig.6 : 32 point kernel functions with unit circle scaled by 4

6. SIMULATION RESULTS:

Testing of The Multibit FFT algorithm is first tested using Matlab program. The program will simulate all possible simultaneous conditions like

(i) Two Continuous Wave (CW) signals.
(ii) Two pulsed signals for various pulse widths.
(iii) One CW and one Pulse signals

Frequency of the input signal will be limited to 750 – 1250 MHz zone. Random noise is also added with the signal and its impact on signal detection presence will also be presented.

6.1 Two Continuous Wave Signals:

The two simultaneous continuous wave signals given as the input to the radix 2 FFT module mathematically represented

s= A1 sin(2*pi* f1*t)+ A2 sin(2*pi* f2*t)
Here,
A1 & A2 =1 unit are the amplitude of two signals
f1 & f2 are the frequencies of the two signal

Simulations using Matlab:

CW on CW ; f1 = 800Mhz, f2= 900Mhz

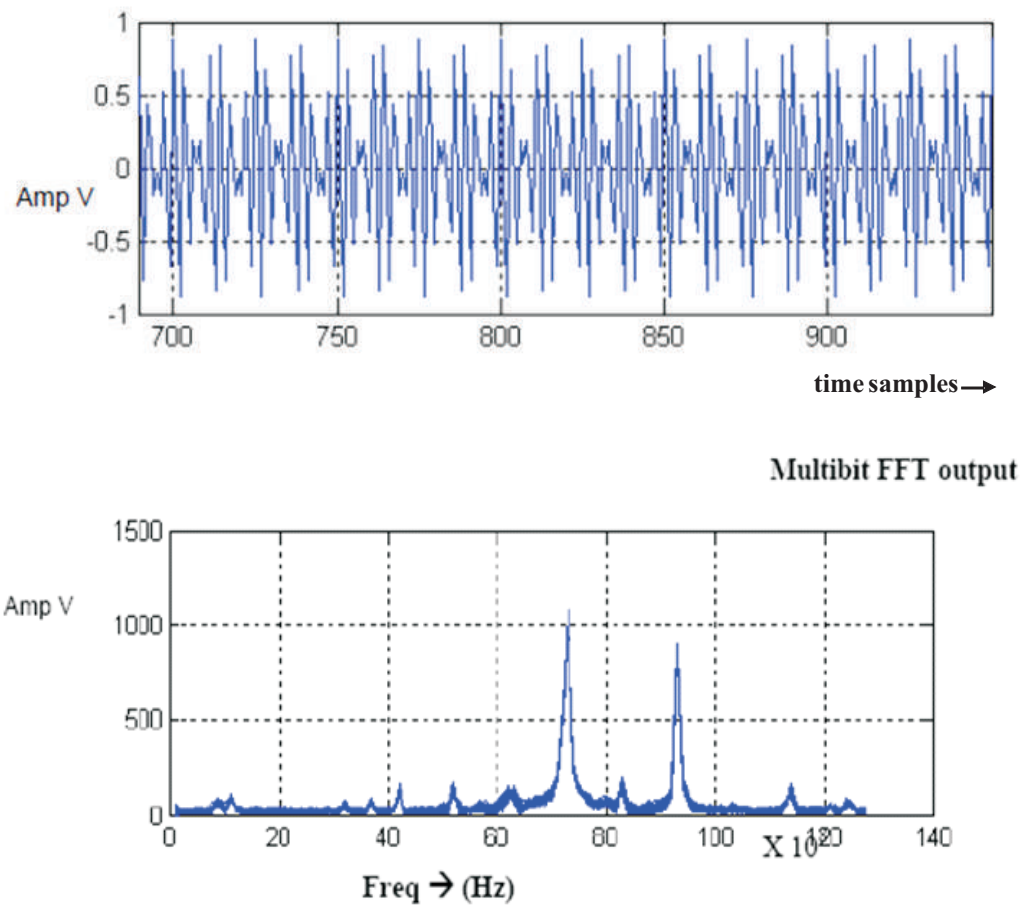

Fig. 7: plot for two continous wave (CW) signals

6.2 Two pulse signals Matlab plot:
Pulse on pulse :f1=800mHz f2=1100mHz

Pulse on Pulse ; f1 = 800Mhz, f2= 1100Mhz

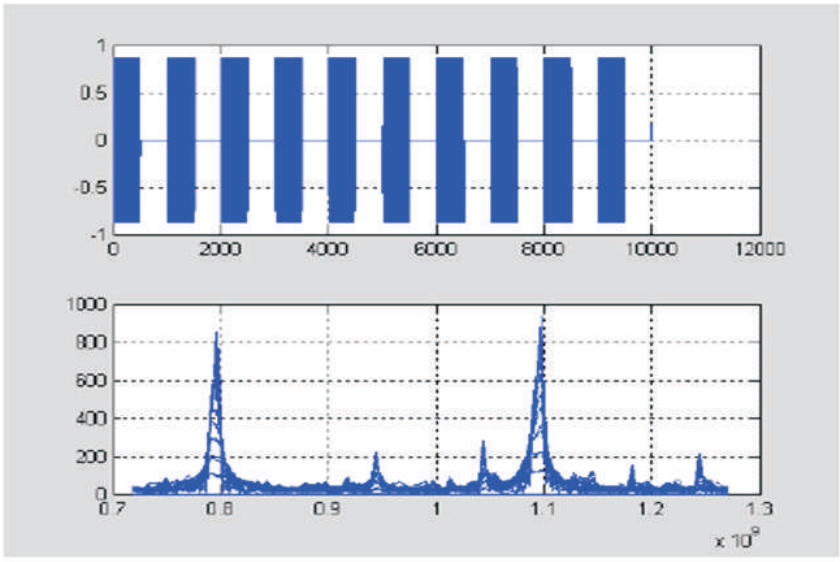

Fig.8: plot for two pulse signals

6.3 one continuous& one pulse signal:

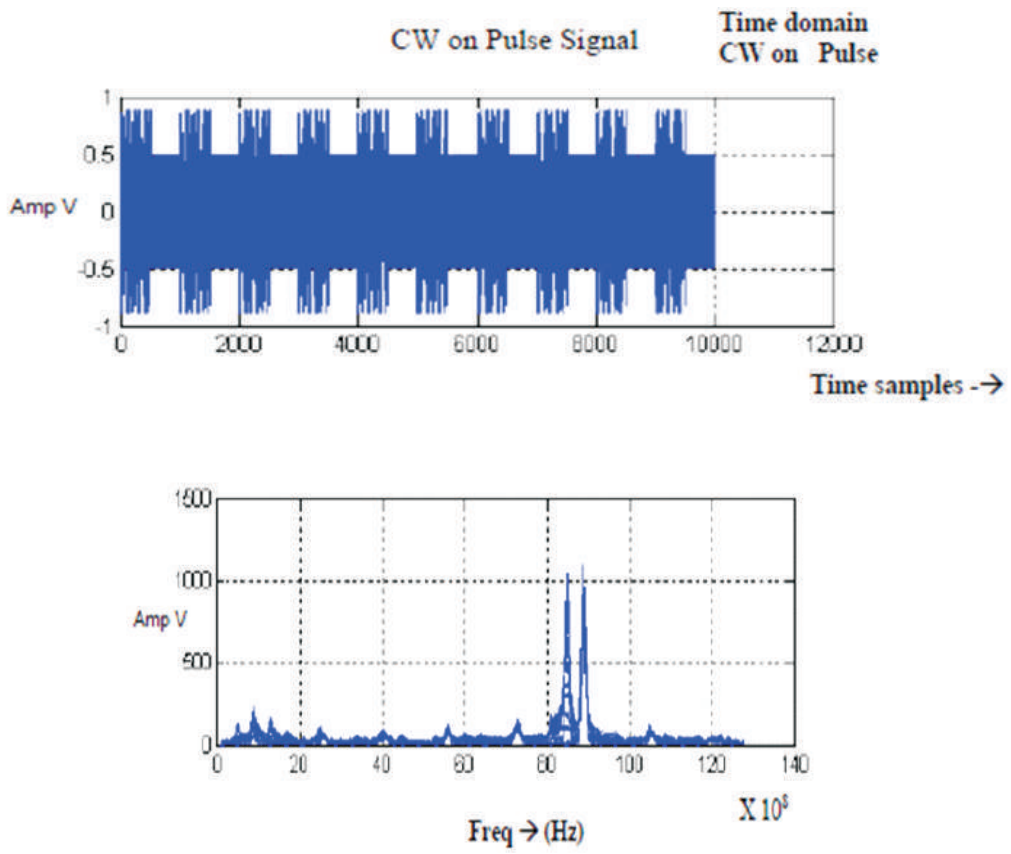

Fig.9:Plot for CW on pulse signal

From the Matlab plots, for finding the first peak, the bins corresponding to the frequency of the signal given at input and its adjacent bins on either side are compared. The highest among these three bins is noted as the first peak (peak1). Similarly, we find the second peak (peak2) by comparing the 3 bins around the frequency corresponding to the second signal. Next we determine the value of spur which is the highest value among the remaining bins(4). The bins corresponding to the two signals and their adjacent bins on either sides are excluded. Now we compare the values of peak1 and peak2with the value of spur.

In multibit plot peak1 value code is 1200 & peak2 value is 900 and the value of spur is 250.

V1 =>20 log(peak1/ spur) = 20 log(1200/250) =20 log(4.8) = 13.62 dB
V2 =>20 log(peak2/ spur) = 20 log (900/250) =20 log (3.6)= 11.1 dB

In monobit plot peak1 value code is 225 & peak2 value is 180 and the value of spur is 70.

V1 =>20 log(peak1/ spur) = 20 log(225/70) =20 log(3.2) = 10.1 dB
V2 =>20 log(peak2/ spur) = 20log(180/70) =20 log (2.5)= 7.9 dB
V1 & V2 are the dynamic ranges calculated based on the matlab plots.

With more number of kernel point approximations the noise is reduced and the instantaneous dynamic range is increased by 3 to 4 dB in the multibit receiver when compared to monobit receiver,as is given in above calculations and in the plots . The noise is suppressed in the multi-bit and hence rounding error is reduced.

From the above plots, the design of the multi bit receiver with the use more number of kernel pointsshowed better results such as fine frequency resolution, good frequency accuracy, reduced noise and improved dynamic range..

7. CONCLUSION:

The Digital Receiver discussed here includes advance feature from microwave and digital domain for designing a frequency receiver to get higher accuracy, good dynamic range, high sensitivity, modular and lower cost and it also exploits breakthrough in ADC technology and FPGA .However, the problem of simultaneous signal remain a problem of DIFM receiver which is being solved using this digital receiver. These digital receivers are will suited to perform as wide band Channelizer, tunedsuperheterdyne receiver, compressive receiver functions. Particularly these types of receivers used in radar EW applications.

The Monobit Digital Receiver is capable of processing simultaneous signal with good frequency accuracy along with Pulse Width(PW) and Time–of-Arrival (TOA) measured data on pulse by pulse basis.. After a thorough testing the hardware for a digital receiver a Multi Chip Module (MCM) can be created which can include IF section, Sampling, and processing algorithms. The Monobit concept can also be extended to analyze the low probability of intercept signals by suitably developing the different algorithms.

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