ORIGINAL ARTICLE ISSN:-2230-7850

Indian Streams Research Journal

Abstract:-

Basic logic gates are the fundamental building blocks of logic design . These logic gates are used to design combinational logic circuits for various practical applications. Sequential logic circuits have been designed by incorporating various memory elements to the existing combinational logic circuits. Applications of Probability concepts have been mingled with our day-to-day real life operations. Probability applications are inevitable in domains wherever there is an uncertainity. Probability rules the roost over all existing uncertainity domains. Here in this paper an attempt is made to represent (show) that various problems of probability can have logic gates' solutions and similarly various logic gate problems can have probabilistic solutions.

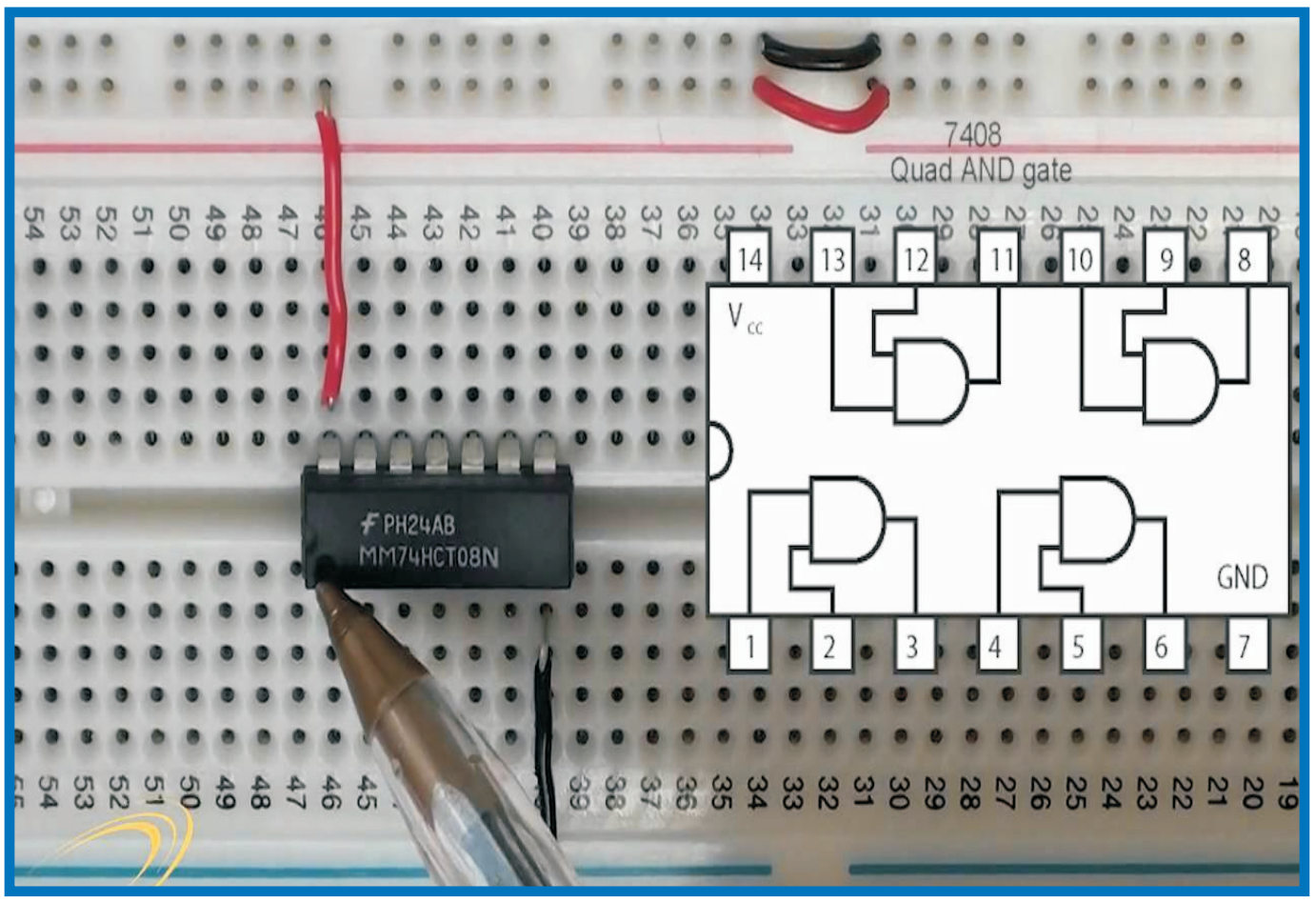
D. V. S. S. Subrahmanyam

Principal , Rishi M.S.Institute of Engg. & Tech. For Women, Near Jntu-H, Kukatpally, Hyderabad .

PROBABILITY APPROACHES TO BASIC LOGIC GATES

Keywords:

Logic gates , NOT , OR , AND , NAND , NOR , XOR , XNOR , Probability.



INTRODUCTION:

Logic gates are building blocks to the entire domain of digital logic gates. These are NOT, AND , OR , NAND (AND + NOT) , NOR (OR + NOT) , XOR (EXCLUSIVE OR) , XNOR (EXCLUSIVE NOT OR) gates. Among these NOT , AND and NOR are called BASIC GATES / FUNDAMENTAL GATES. NAND and NOR gates are applications of AND and OR Gates respectively .The remaining gates are Exclusive gates. Each gate has its own course of action and applications.

(OR + NOT) , XOR (EXCLUSIVE OR) , XNOR (EXCLUSIVE NOT OR) gates. Among these NOT , AND and NOR are called BASIC GATES / FUNDAMENTAL GATES. NAND and NOR gates are applications of AND and OR Gates respectively .The remaining gates are Exclusive gates. Each gate has its own course of action and applications.

Digital Logic design is entirely based on the concept of High / Low inputs of variables. If voltage is High then it is represented as 1 , if voltage is Low then it is represented as 0. These High / Low can also be referred as ON / OFF respectively. If the voltage of any input variable is HIGH i.e., 1 then that variable enters into the circuit. If the voltage of any variable is LOW i.e., 0 then that variable does not enter into the circuit. Thus the status of any variable is represented either by 1 or 0. Thus all inputs and outputs are in terms of 0s and 1s only. Any logic circuit is basically a group of many logic gates . Various number systems are used in logic design. But all these number systems are represented in 0s and 1s only. Here the main point is to say that basically Digital Logic Design is based on two numbers i.e., 0 and 1.

Probability deals with both discrete and continuous random variables. Here Probability concepts with Discrete nature are only considered for applying them to Digital Logic Design. Thus it is very clear that wherever applications of Logic Design and Probability are considered , these are all discrete in nature.

An experiment can have any number of events, with the following rules :

1.Probability of every event ≥ 0 .

2 Sum of Probabilities of all events = 1

$\sum$ Pi = 1 , where i= 1, 2 , 3 …….. n

3.Number of all events is many but finite.

Probability cannot be represented in negative values .

The actual intention of this paper is to show that a very close relation is existing between Digital Logic Design concepts and Probability fundamental concepts.

Another important note is Digital Logic Design is based on 0 and 1only and Probability values of events can be any number between 0 and 1 including end points. Here every concept is viewed in terms of both Logic Design and Probability.

Discussion . 1 : NOT Gate

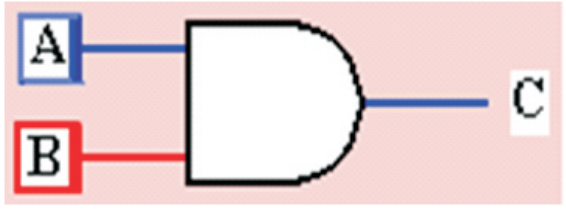
Logic Design : If A is an input to a NOT gate then output is its compliment.

i/p voltage	o/p voltage
High (=1)	Low(= 0)
Low(=0)	High(= 1)

Table : 1.1

Probability : If an event A happens then its Probability is 1. Then Probability of its compliment is 0. Similarly if an event never happens then its Probability is 0. Its compliment is that event happens certainly. i.e., its Probability is 1. Both these concepts yield the same o/p, which is clear from the Table 1.1.

Discussion .2 : AND Gate



C = A . B

Logic Design : If both the inputs are High then o/p is also High. i.e., 1.1=1 , If at least one of the i/p is Low or both i/p are Low then o/p is Low.

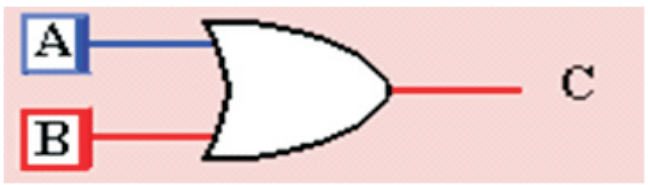
i/p voltage A	B	o/p **voltage**
Low(=0)	Low(=0)	Low(= 0)
Low(=0)	High(=1)	Low(= 0)
High(=1)	Low(=0)	Low(= 0)
High(=1)	High(=1)	High(= 1)

Table : 1.2

Probability : If A and B are two independent events and Prob (A) = p and Prob (B) = q then
Probability when event A never happens and event B never happens = 0 * 0 = 0….(1)
Probability when event A never happens and event B happens = 0 * q = 0…….(2)
Probability of event A is to happen and event B never happens = p*0 = 0 ……(3)
Probability of event A is to happen and event B is also to happen = p* q = p. q ……..(4)
It is very clear that the o/p of the above three events (1),(2),(3) are as same as the o/p voltages of the above Table 1.2.
But for the result (4) it is different . Here Logic Design concept cannot directly be applied. Because in Logic Design (Boolean Algebra) , when both inputs are High implies product of two one's is one i.e., product of two Highs is also High. But in Probability concept, it is multiplication of two Probability values which is again a Probability value. i.e., it certainly happens.

Discussion . 3: OR Gate

Logic Design : If at least one of the i/p voltage is High then o/p is also High. If both the i/p are Low then o/p is also Low.



C = A + B

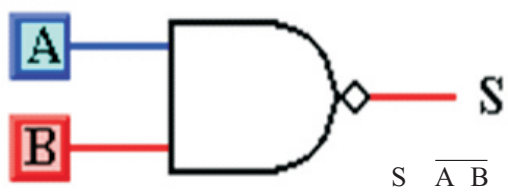
i/p voltage A	B	o/p **voltage**
Low(= 0)	Low(= 0)	Low(= 0)
Low(= 0)	High(= 1)	High(= 1)
High(= 1)	Low(= 0)	High(= 1)
High(= 1)	High(= 1)	High(= 1)

Table : 1.3

In Boolean Algebra sum of two Highs is also High. i.e., 1+1=1 (Last row of the above Table)

Probability :
Probability when event A never happens or event B never happens = 0 + 0 = 0 …..(5)
Probability when event A never happens (or) B is to happen = 0 + q = q …….(6)
Probability of A is to happen (or) B never happens = p + 0 = p ……(7)
Probability of A is to happen (or) B is to happen = p + q ……(8)
It is very clear that the o/p of the above three events (5), (6), (7) are as same as the o/p voltages of the above Table 1.3.
But for the fourth one (8) it is not directly related. In Probability, sum of two Probability values gives another Probability value i.e., it certainly happens.

.Discussion . 4: NAND Gate



Logic Design : This Gate gives an o/p that is compliment of the o/p of an AND gate.

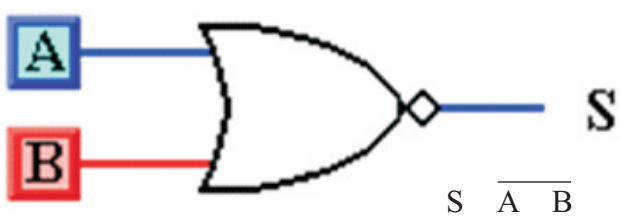
NAND Gate = AND Gate + NOT Gate

i/p voltage A	i/p voltage B	o/p voltage
Low(=0)	Low(=0)	High(= 1)
Low(=0)	High(=1)	High(= 1)
High(=1)	Low(=0)	High(= 1)
High(=1)	High(=1)	Low(= 0)

Table : 1.4

Probability : If A and B are two events ,
Then (From Discussion 2)
Probability of not to happen event (1)
is = { 1-0 } = 1 …….(9)
Probability of not to happen event (2)
= { 1- 0 } = 1 ……(10)
Probability of not to happen event (3)
= { 1- 0 } = 1 ……..(11)
Probability of not to happen event (4)
= { 1 - p* q } = 1-p.q ……(12)
It is very clear that the o/p of the above three events (9),(10),(11) are as same as the o/p voltages of the above Table 1.4.
But for the fourth condition (12) , it differs from the basics of Digital Logic Design. Because there are only two o/p in Logic
Design either 1 or 0 i.e., High or Low. But in Probability , there are many o/p between 0 and 1.

Discussion . 5: NOR Gate



NOR Gate = OR Gate + NOT Gate
Logic Design : This Gate gives an o/p that is compliment of the o/p of an OR gate.

i/p voltage A	i/p voltage B	o/p voltage
Low(= 0)	Low(= 0)	High(=1)
Low(= 0)	High(= 1)	Low(= 0)
High(= 1)	Low(= 0)	Low(= 0)
High(= 1)	High(= 1)	Low(= 0)

Table 1.5

Probability :
(From Discussion 3)
Probability of not to happen event (5)
= { 1 - 0 } = 1 ……..(13)
Probability of not to happen event (6)
= { 1 - q } ……..(14)
Probability of not to happen event (7)
= 1 – p…….(15)
Probability of not to happen event (8)
= 1 – { p+ q }……(16)
It is very clear that the o/p of the above event (13) is as same as o/p of the first event in the Table 1.5.
But remaining events (14), (15) and (16) have indirect relations to the above concepts of Logic Design.
Because there are only two o/p in Logic
Design either 1 or 0 i.e., High or Low. But in Probability , there are many o/p between 0 and 1.

Discussion . 6: XOR Gate

Logic Design : It is an Exclusive OR gate.

i/p voltage A	B	o/p **voltage**
Low(= 0)	Low(= 0)	Low(=0)
Low(= 0)	High(= 1)	High(= 1)
High(= 1)	Low(= 0)	High(= 1)
High(= 1)	High(= 1)	Low(= 0)

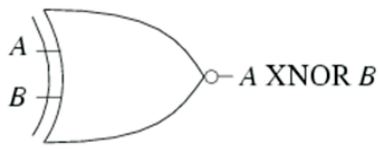
Table : 1.6

If both the i/p are either Low or High then o/p is Low. But if one i/p is High and another i/p is Low then o/p is High.

Probability : A and B are two events to hit a particular target. If both are trying to hit the target then chance for A to hit the target is Chance for B to hit the target is Thus Probability to hit the target either by A or by B is , which is as same as the o/p of the above gate .

Discussion . 7: XNOR Gate

Logic Design :



A XNOR B = =

XNOR Gate = XOR Gate + NOT Gate.

i/p voltage A	B	o/p **voltage**
Low(= 0)	Low(= 0)	High(=1)
Low(= 0)	High(= 1)	Low(= 0)
High(= 1)	Low(= 0)	Low(= 0)
High(= 1)	High(= 1)	High(= 1)

Table : 1.7

If both the i/p are either Low or High then o/p is High. But if one i/p is High and another i/p is Low then o/p is Low.

Probability : A and B are two events to hit a particular target. If both are trying to hit the target then chance for both A and B to hit the target is A.B. And chance for both A and B not to hit the target is (neither of them should hit the target) . Probability that either both should hit the target or both should not hit the target is which is the o/p of an XNOR Gate, which is represented in the above Table 1.7.

CONCLUSIONS :

In the same way many other relations can also be discussed and applied for advanced concepts. The mapping between Logic Design and probability concepts is not one to one. But here the main attempt is to get an one to one mapping between a maximum number of Probability applications and Digital Logic Design concepts.

REFERENCES :

1.Alan Clements, Principles of computer hardware. second edition oxford science publications.
2.M. M. Mano, Digital Design, Prentice Hall.